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Design and Control of STATCOM using Modular Multilevel Converters for Voltage Profile Enhancement in Distribution Systems

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Declaration

I declare that this thesis titled "Design and Control of STATCOM using Modular Multilevel Converters for Voltage Profile Enhancement in Distribution Systems" is the result of my own research except as cited in the references. It is being submitted to the Master's Degree in Electrical Engineering from the Faculty of Engineering and Technology at Birzeit University. Palestine. This thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree

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Abstract

This thesis proposes a new modular multilevel conversion system with integrated capacitors for STATic synchronous COMpensator (STATCOM) applications. The new converter is called a Single Star-Modular Multilevel Converter (SS-MMC). In our proposed converter, the capacitors are connected in series via half bridge chopper circuits to order to separately discharge and recharge each capacitor. The projected converter is able to compensate the reactive power to the loads and improve the grid's power factor. The converter is controlled using a decoupled direct and quadrature current controller with a phase locked loop controller. The proficiency and functionality of the proposed converter with its controller are demonstrated through detailed theoretical analysis and simulations with MATLAB/Simulink.

المستخلص

تقترح هذه الأطروحة نوعا جديدا من القلابات متعدد المستويات مع مكثفات مقحمة لتطبيقات معوض الطاقة الخيالية المتزامن الثابت (STATCOM). في هذا النظام الجديد، يتم توصيل المكثفات في سلسلة من خلال محول نصف حلقة لتفريغ وإعادة شحن كل مكثف على حدة. القلاب المقترح قادر على تعويض الطاقة الخيالية للأحمال وتحسين معامل قدرة الشبكة. يتم التحكم في القلاب باستخدام وحدة تحكم طاقة حقيقية وخيالية منفصلة مع وحدة تحكم حلقة مغلقة الطور. يتم إظهار كفاءة ووظيفة المحول المقترح مع وحدة التحكم الخاصة به من خلال التحليل النظري المفصل والمحاكاة باستخدام برنامج المحاكاة MATLAB / Simulink.

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Chapter 1

Introduction

Recently, with the increased popularity of static and dynamic inductive loads with the application of power electronic devices in modern industries, some large inductive loads cause problems in power quality [1], [2]. The problems appear in electric grid as increased harmonics and low power factors. The capacity of the electric distribution system and power losses are affected by the presence of harmonics and low power factor operation [2], [3].

1.1 Problem Statement

The effect of nonlinear and/or inductive loads on the power factor is an important issue for the operation of the power system and attracts the interest of many researchers. Many research papers have proposed different schemes to improve power quality in the presence of nonlinear and/or inductive loads [4]. The STATic synchronous COMpensator (STATCOM) is one of the convertors that is able to improve the power quality and mitigate disturbance [5]-[7]. The STATCOM usually includes two-level voltage/current source inverter with a line-frequency transformer added for the enhancement of its power ratings; however, it results in the heavy, unreliable and expensive design of the STATCO [5],[6]. Moreover, the two-level inverter produces output line voltages with a substantial harmonic content. Therefore, in order to extract the fundamental components of the inverter output waveforms, filters should be added [8]. The reliability of this two-level inverter is relatively low and is independent of the amount of generated reactive power. If one of the switches is faulty, the two-level inverter becomes unable to generate a reactive power to the load [8]. These

restrictions necessitate the use of multilevel converters or modular multilevel converters (MMC) to eliminate the use of transformer and reduce the harmonic contents of the output waveforms of the converter, which makes the design of filters easier and simple.

The most popular multilevel converters employed in STATCOM applications are Flying-Capacitor Multilevel Converters (FCMCs) and Diode-Clamped Multilevel Converters (DCMCs) [9]. The low reliability in both topologies, the high cost of flying capacitors in FCMC, as well as the need for a complicated capacitor voltage balancing controller in DCMC are considered as the major disadvantages of these two topologies.

On the other hand, the most popular modular multilevel converters employed in STATCOM applications are Cascaded H-bridge Multilevel Converters (CHMCs) and Double Star-Modular Multilevel Converters (DS-MMC) [9]-[11]. These topologies are providing high voltage transformer-less structures with an improved efficiency, reliability, and fault tolerance capability [12]. Therefore, the CHMC and DS-MMC configurations seem to be more suitable among others such as FCMCs and DCMCs.

This thesis presents a new STATCOM, called Single-Star Modular Multilevel Converter (SS-MMC). The proposed topology is believed to offer many advantages [12]:

- The output Voltage produced by this convertor is with very low harmonics, which makes the requirement of filter design simple and cheap.
- The converter's leg can be used in the case of damaged chopper circuits since the damaged modules can be easily replaced by new modules.
- If the output voltage is required to be increased, additional chopper circuits can be easily added to the converter's leg to increase the magnitude of the output voltage and decrease the Total Harmonic Distortion (THD) in the output voltage.

- The converter is able to individually charge and discharge the capacitors, which simplifies adding a capacitor-voltage balance controller to balance the capacitors in terms of their voltages.
- The converter can be modulated using a low switching frequency, which results in a higher efficiency.
- The converter has a higher reliability for a wide range of reactive power generation compared with the traditional 2-level inverter.

The main contribution of this thesis is to model, control and simulate a new modular multilevel converter with embedded capacitors, which is able to compensate the reactive power to the loads and improve the grid's power factor.

In comparison with the DS-MMC, the proposed converter has half the number of switches with no injected circulating currents. The converter has no buffer inductors due to the absence of circulating currents and, consequently, reduced conduction losses; this allows the converter operation at a higher efficiency. Moreover, the use of SS-MMC eliminates the need for arm balancing control, which is necessary in the control strategy of the DS-MMC to balance the top and bottom arms within the same leg. The converter needs twice the number of modules compared to the SS-MMC in order to produce the same output voltage.

In comparison with the CHMC, which is also a single star modular multilevel converter where each leg is implemented by a series connection of H-bridge converters [13], the proposed converter is more reliable and it is designed using half the number of switches.

1.2 Research Goals

Following are the main goals and objectives of this thesis:

- Explain the circuit diagram and operating principle of the proposed converter
- Develop a comprehensive mathematical model for the converter's controller to generate the appropriate reactive power
- Demonstrate the operation of the converter through detailed theoretical analysis and numerical simulations using MATLAB/Simulink
- Examine the converter's current controller with grid synchronization
- Examine the capacitor balancing based on applying capacitor voltage-balancing controllers considering the operating conditions with non-equal voltages of the capacitors
- Confirm that the new conversion system can be used to compensate the required reactive power to the load and make the grid operate at nearly a unity power factor.

1.3 Organization of The Report

The report comprises six chapters that are organised as follows:

- Chapter (2) reviews some converters used for STATCOM applications summarizing their advantages and disadvantages.
- Chapter (3) describes the structure, the principle of operation, and the mathematical model of this new converter.
- Chapter (4) demonstrates the control system of the proposed converter including, reactive power controller, capacitor voltage balancing controller, and the grid synchronization.
- Chapter (5) presents simulation results of the proposed converter in different scenarios.
- Chapter (6) presents the conclusion of the research work and suggests possible future works.

Chapter 2

Literature Review

The chapter presents review and comparisons between STATCOM topologies focusing to summarize their advantages and disadvantages. The comparison has been carried out according to circuit design, voltage/current stress, complexity, harmonics, size, cost, etc ….

2.1 Two-Level Inverters

The topology of the two-level inverter, being the most straightforward, is used to compensate the reactive power. The circuit diagram of the two-level inverter topology presented in Fig. 2.1 accompanied by the line output voltage between phases *a* and *b*. The converter consists of three legs where each leg consists of top and bottom switches with their two anti-parallel diodes. In order to avoid the short circuit across the DC link, the switches are controlled in a complementary way. So as to generate the required AC voltage waveform, the inverter moves from one valid state to another in order to form two-level output voltage. Thus, the output phase voltages with respect to the virtual neutral point has two values that are $\pm\frac{1}{2}V_{dc}$ creating two levels. In addition, the output line voltages have three levels that are $\pm V_{dc}$ and 0 as also shown in the same figure. The selection of the switching states is done by a modulation technique in order to generate the levels of the output voltage [8].

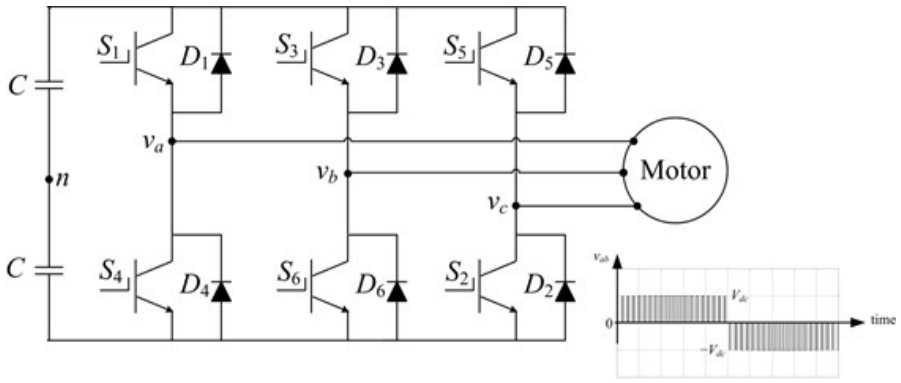

Fig. 2.1: The structure of the two-level [18]

The two-level inverter ‘s main advantages are summarized as follows:

- The converter is easy to be experimentally implemented.
- The converter’s control system is simple.
- The voltage and current stresses are equally distributed on the switching devices.

The major disadvantages of the two-level inverter are presented as below:

- The converter produces an output line voltage with significant harmonics.
- The converter is usually modulated at high switching frequency.
- The converter has a low reliability.

2.2 Diode Clamped Multilevel Converters (DCMCs)

Fig. 2.2 illustrates the circuit diagram of the four-level DCMC with the waveform of the four-level line voltage. The converter has three legs and each leg is designed to include six switches with six anti-parallel diodes, and four clamping diodes. Moreover, the main DC link of the converter is connected to three capacitors. The switches in the top and bottom arms within the same leg are controlled in a complementary way.

The resulting AC output phase voltages, v_{ao}, has four levels of voltages that are V_{dc}, $\frac{2}{3}V_{dc}$, $\frac{1}{3}V_{dc}$

and 0 and the resulting AC output line voltages has four positive levels of voltages that are V_{dc}, $\frac{2}{3}V_{dc}$, $\frac{1}{3}V_{dc}$ and 0 as indicated in Fig. 2.2 [8], [14], and [15].

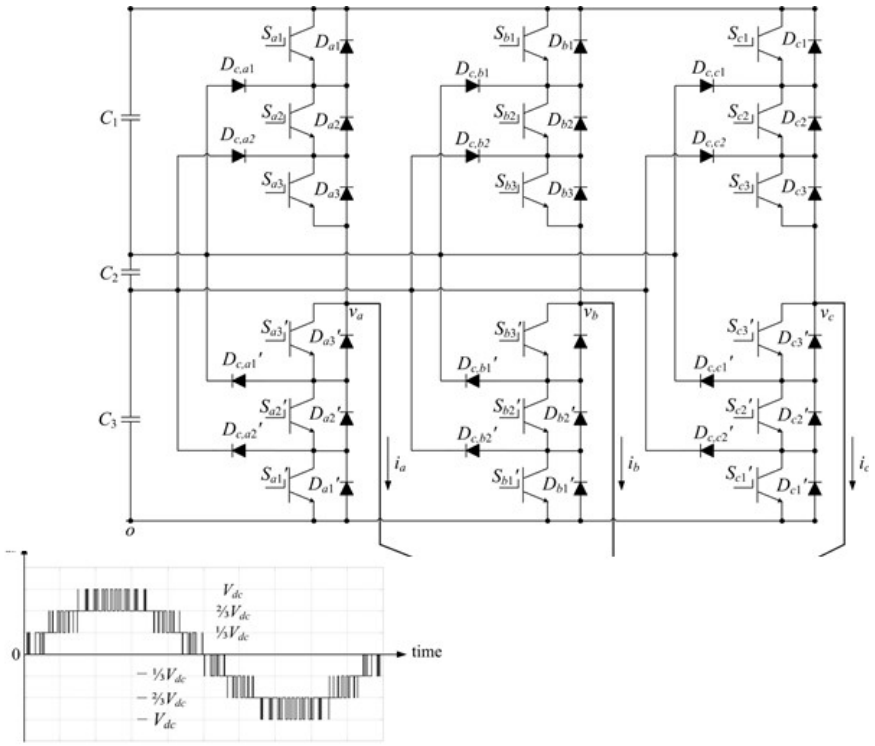

Fig. 2.2: The structure of the four-level DCMC [18]

The major advantages of the DCMC can be summarized as follows:

- The output voltages and currents have a lower THD compared to two level inverter.
- The converter operates at low switching losses with higher efficiency.
- The voltage stress on the switches is also significantly smaller.
- The control method of the converter is relatively simple.

Following is a summary list of the main disadvantages of the DCMC

- The clamping diodes and switching devices have unequal ratings.
- Increasing the number of output voltage levels would increase the complexity of the DCMC.

- The implementation of the converter is complicated for a high number of levels.
- The capacitor voltages are unbalanced and require a balancing controller.

2.3 Flying Capacitor Multilevel Converters (FCMCs)

This topology uses clamping capacitors instead of clamping diodes. Fig. 2.3 illustrates the circuit diagram of the four-level FCMC along with the line voltage, v_{ab}. The converter consisting of three identical legs where each leg is designed to include six switches with their anti-parallel diodes, and three additional clamping capacitors producing four levels of line voltages. The switches in the top and bottom switches within the same leg are controlled in a complementary way and the function of the capacitors is to clamp the switch voltages to $\frac{1}{3}V_{dc}$. The output voltages of FCMC Convertor and the DCMC inverter are very similar. However, the FCMC offers more switching states than the DCMC. This redundancy makes the control of capacitor voltages to be more flexible [8], [14], and [15].

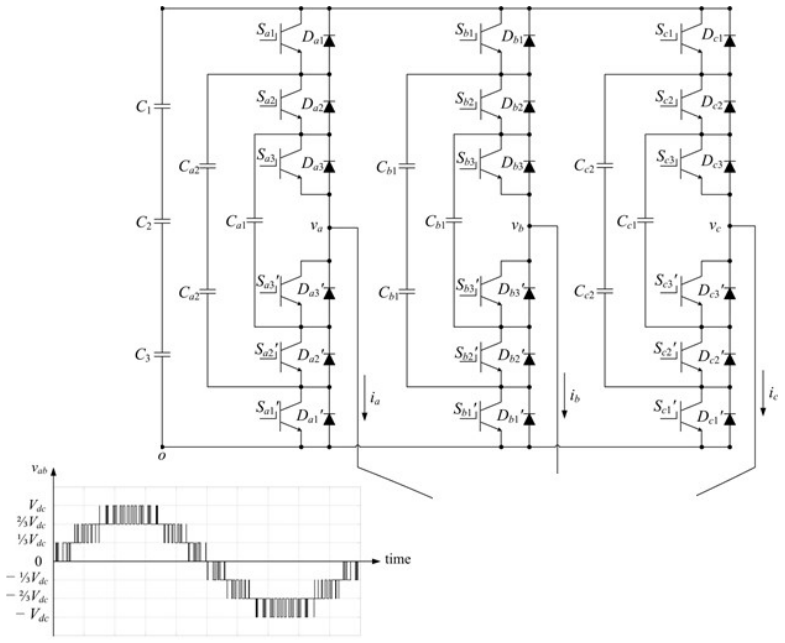

Fig. 2.3: The structure of the four-level FCMC [18]

The major advantages of the FCMC can be summarized as follows:

- The output voltages and currents have a lower THD compared with the two-level-inverter.
- Having a large amount of storage capacitors, in case of the failure of one level of the structure, the converter is able to keep operation.
- The FCMC provides switch combination redundancy to balance the capacitor voltages.
- The voltage stress on the switches is substantially smaller compared with the two-level-inverter.

The FCMC major disadvantages can be listed as below:

- The FCMC requires excessive number of storage capacitors when increasing the number of levels.
- Having bulky power capacitors makes it very expensive and very hard to be implement.
- The control system can be very complicated.

2.4 Cascaded H-bridge Multilevel Converters (CHMCs)

This converter consists of three identical legs in which each leg is designed using a series connected H-bridge (full bridge) converters with floating capacitors. Fig. 2.4 illustrates the circuit diagram of a three-phase CHMC, where the output voltage across the leg is the sum of the output voltages produced by the H-bridge converters. Three different output voltages, $\pm V_{dc}$ and zero are generated by each bridge; depending on the switching states of the switches S_1, S_2, S_3, and S_4 [8], [14], [15]. The converter will produce (n + 1)-voltage levels in the line voltage when connecting n series full bridge convertors in a leg.

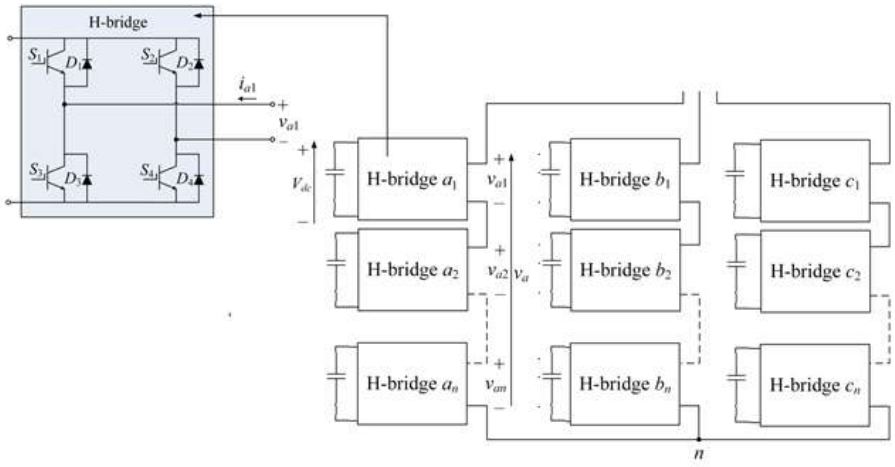

Fig. 2.4: The structure of the CHMC [18]

The major advantages of the CHMC can be summarized as follows:

- The output voltages and currents have a lower THD compared with the two-level-inverter.
- The topology requires less number of devices to produce the same number of voltage levels compared with the DCMC.
- Modularity design and this enables the manufacturing process to be done more quickly and cheaply.
- The H-bridges have equal ratings.

The CHMC major disadvantages can be listed as below:

- High conduction losses.
- The capacitor voltages are unbalanced and require a balancing controller between the capacitor voltages to make the voltage stress distributed equally across the capacitors.

2.5 Double-Star Modular Multilevel Converters (DS-MMCs)

The converter consists of three identical legs and each leg consists of top and bottom arms.

Each arm comprises a series of connected half-bridge converters in which each half-bridge is associated with a separate capacitor. Fig. 2.5 illustrates the circuit diagram of a three-phase DS-MMC where the output voltage is the sum of the outputs of the half-bridge converters. The top and bottom arms are connected to each other via buffer inductors to limit the circulating current in the converter. With the different combinations of the two switches, S_a and S_m, each half bridge would generate two output voltages, V_{dc} and zero [16]-[18]. The converter produces $(n + 1)$-voltage levels in the line voltage when including n series half bridge chopper cells in each arm.

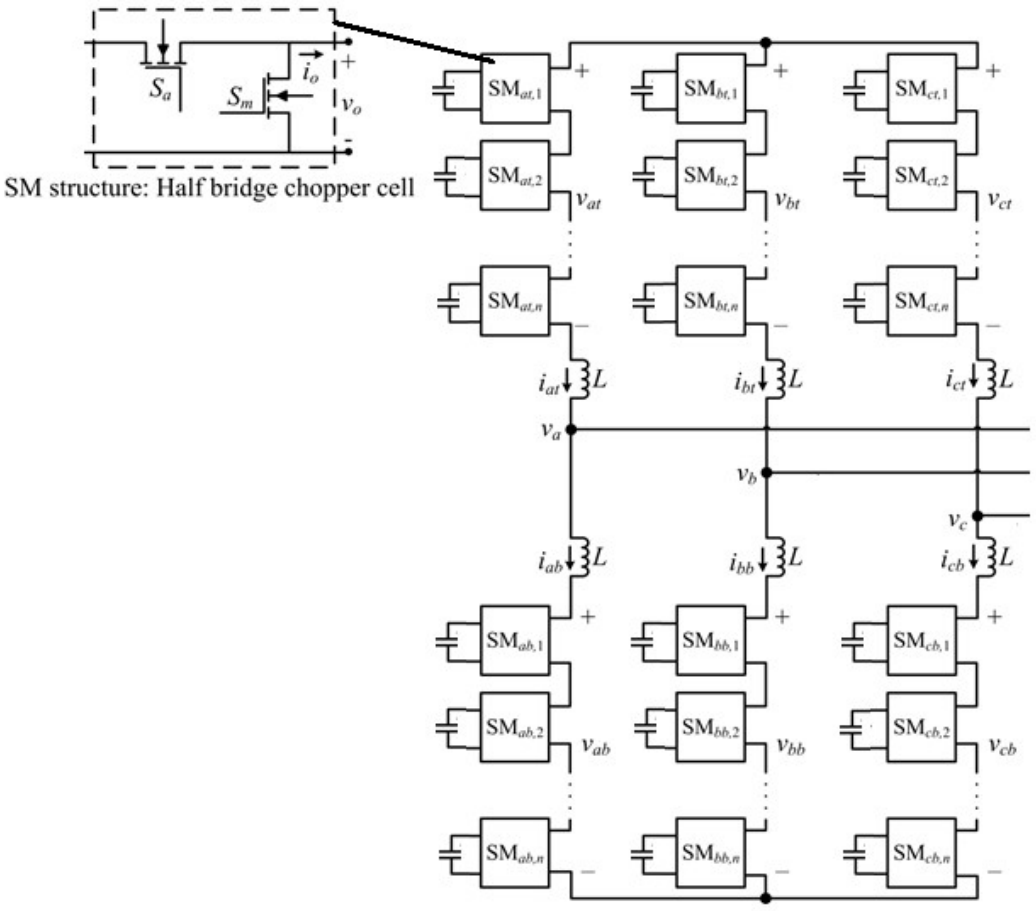

Fig. 2.5: The DS-MMC circuit diagram

The advantages and disadvantages of the DS-MMC are similar to that of CHMC. However, the size and cost of this topology are higher due to the use of buffer inductors and the topology requires an additional circulating current controller. Moreover, this circuit needs an arm-balancing controller to achieve the balance between the top and bottom arms within the same leg [16]-[18]. To overcome these problems, a new modular multilevel converter (SS-MMC) is recommended for STATCOM applications. The proposed converter has no buffer inductors due to the absence of circulating currents and, consequently, reduced size and weight. Moreover, the use of this converter eliminates the need for arm balancing control, which is necessary in the control strategy of the DS-MMC to balance the top and bottom arms within each phase

Table 2.1 lists, compares and summarizes the advantages and disadvantages of all discussed topologies included in Chapter 2

Table 2.1: Advantages and disadvantages between topologies.

Topology	Advantages	Disadvantages
Two level Inverter	• Easily implemented • Simple control system • Equal voltage and current stresses	• High THD • High sw. frequency • Low reliability
DCMC	• Low THD • Lower sw. frequency • Small voltage stress • Simple control method	• Unequal device ratings • Complex in implementation for high number of voltage levels • Requires capacitor balancing controller
FCMC	• Low THD • Keeps operating even with the failure of one level	• Excessive capacitors are required for high voltage levels

Topology	Advantages	Disadvantages
	• Redundancy • Small voltage stress	• Expensive • Bulky for high levels • Complicated control system
DS- MMC	• Modularity design • Low THD	• Big size and high cost • Requires an additional circulating current controller • Needs an arm-balancing controller
CH- MMC	• Low THD • Less devices to produce the same number of voltage levels compared to the DCMC • Modularity design • Equal device ratings	• High conduction losses • Requires capacitors balancing controller

Chapter 3

Single Star-Modular Multilevel Conversion System (SS-MMC)

In this chapter, the proposed SS-MMC topology, construction and basic principle of operation will be presented and discussed. The chapter also presents the mathematical model of the proposed conversion system and discusses the modulation strategy that will be used to control the converter. Finally, it addresses a method to calculate the reliability of the proposed converter for comparison purposes with the traditional two-level inverters.

3.1 Converter Structure and Principle of Operation

The circuit configuration of the projected conversion system is illustrated in Fig. 3.1. The AC terminals of the proposed converter are connected to the utility grid. The converter is composed of three legs and each leg has cascaded m-identical sub-modules (SMs) or half-bridges such that each SM consists of two active complementary switching devices with a floating capacitor.

The voltage across the j-th SM (j = 1, 2, …, m) within phase k (k = a, b, or, c) is $v_{C,kj}$ when $S_{kj,1}$ is turned on and it is zero when $S_{kj,2}$ is turned on. The two switches included in each SM must operate in a complementary manner. The SM rated voltage is equal to the nominal capacitive voltage. High voltage IGBTs with antiparallel diodes can be used to implement each SM. Table 3.1 summarizes the possible switches states of the SM considering the direction of the capacitor's current [8].

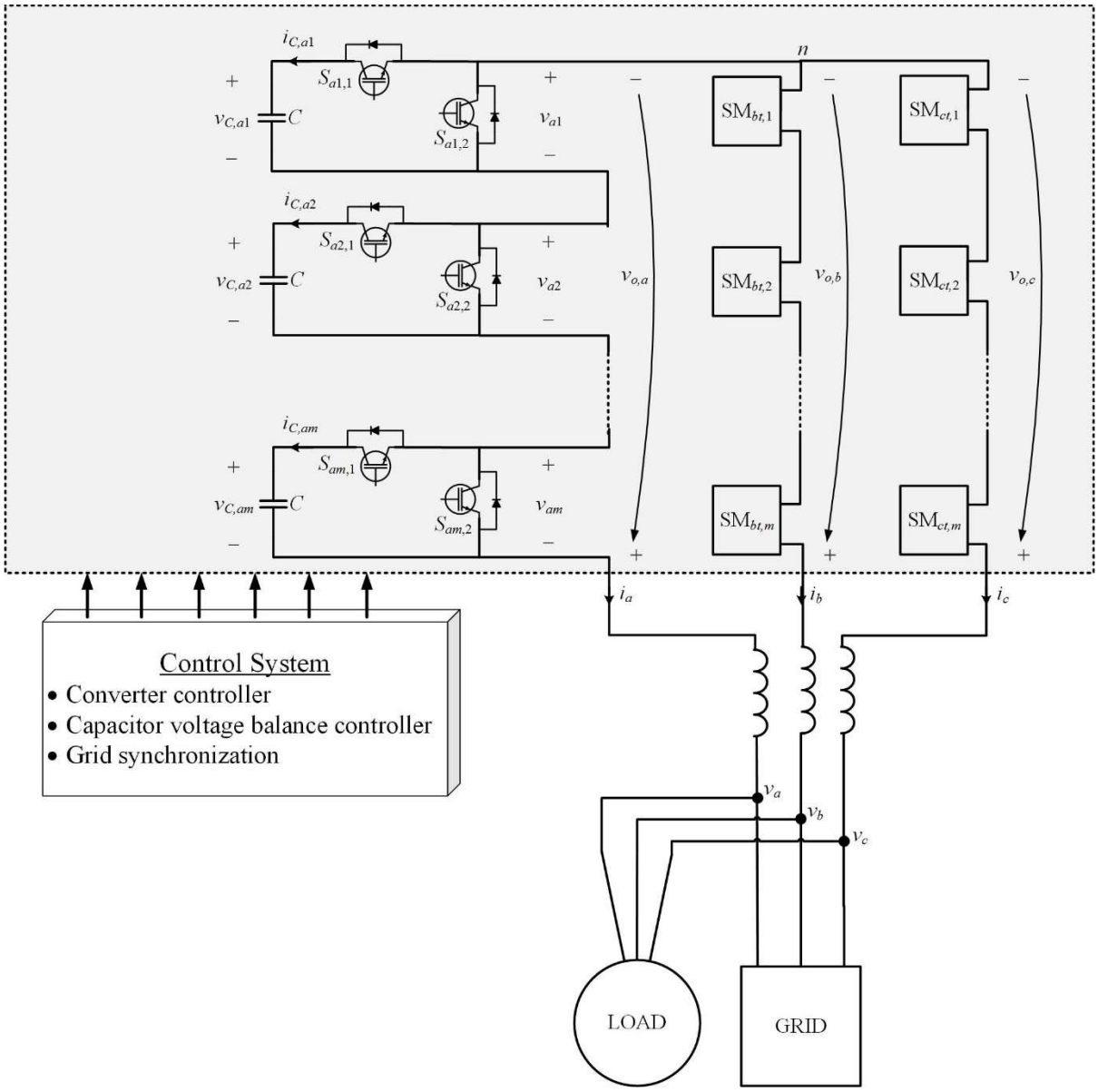

Fig. 3.1: A block diagram of the SS-MMC

Table 3.1: The switch states of the SM

$S_{kj,1}$	$S_{kj,2}$	v_{kj}	current direction	current Path	capacitor's state
1	0	v_c	$i_k > 0$	Diode-$S_{kj,1}$	charging
1	0	v_c	$i_k < 0$	IGBT-$S_{kj,1}$	discharging
0	1	0	$i_k > 0$	IGBT-$S_{kj,2}$	unchanged
0	1	0	$i_k < 0$	Diode-$S_{kj,2}$	unchanged

By switching the half bridges of the switch SMs, each leg is able to generate an adjustable leg voltage with $m + 1$ voltage steps. Assuming that $v_{o,k}$ is the leg's voltage of the generic phase k in reference to n which is the neutral point, being the summation of the voltages of all SM in that leg:

$$v_{o,k} = -\sum_{j=1}^{m} d_{s,kj} v_{C,kj} \tag{3.1}$$

where $v_{C,kj}$ is voltage across the capacitor within the j-th SM in leg k and $d_{s,kj}$ is the switching function of the j-th switch SM in leg k ($d_{s,kj}$ = 1 or 0). The range of the specific leg voltage is

$$-\sum_{j=1}^{m} v_{C,kj} \le \underbrace{-\sum_{j=1}^{m} d_{s,kj} v_{C,kj}}_{v_{o,k}} \le 0 \tag{3.2}$$

Assuming balanced capacitor voltages ($v_{C,kj} = v_C$) with negligible ripples, $v_{o,k}$ can be approximated as:

$$v_{o,k} \approx -v_C \sum_{j=1}^{m} d_{s,kj} = v_k - \frac{m v_C}{2}; \; -\frac{m v_C}{2} \le v_k \le \frac{m v_C}{2}, \tag{3.3}$$

where $v_{o,k}$ is the converter's phase k voltage in reference to N being the grid's neutral point,.

Fig. 3.2 shows the structure of one leg when $m = 3$. Assuming that, the capacitors are balanced and have the same voltage (v_C), then the leg voltage will have 4 levels and these levels are generated as follows:

- When $S_{k1,1}$, $S_{k2,1}$, and $S_{k3,1}$ are turned off, the voltage level is 0
- When $S_{k1,1}$ and $S_{k2,1}$ are turned off while $S_{k3,1}$ is turned on, the voltage level is $-v_C$
- When $S_{k1,1}$ and $S_{k3,1}$ are turned off while $S_{k2,1}$ is turned on, the voltage level is $-v_C$
- When $S_{k2,1}$ and $S_{k3,1}$ are turned off while $S_{k1,1}$ is turned on, the voltage level is $-v_C$
- When $S_{k1,1}$ is turned off while $S_{k2,1}$ and $S_{k3,1}$ are turned on, the voltage level is $-2v_C$
- When $S_{k2,1}$ is turned off while $S_{k1,1}$ and $S_{k3,1}$ are turned on, the voltage level is $-2v_C$
- When $S_{k3,1}$ is turned off while $S_{k1,1}$ and $S_{k2,1}$ are turned on, the voltage level is $-2v_C$
- When $S_{k1,1}$, $S_{k2,1}$, and $S_{k3,1}$ are turned on, the voltage level is $-3v_C$

Table 3.2 Summarizes the possible switch states for the proposed converter when $m = 3$.

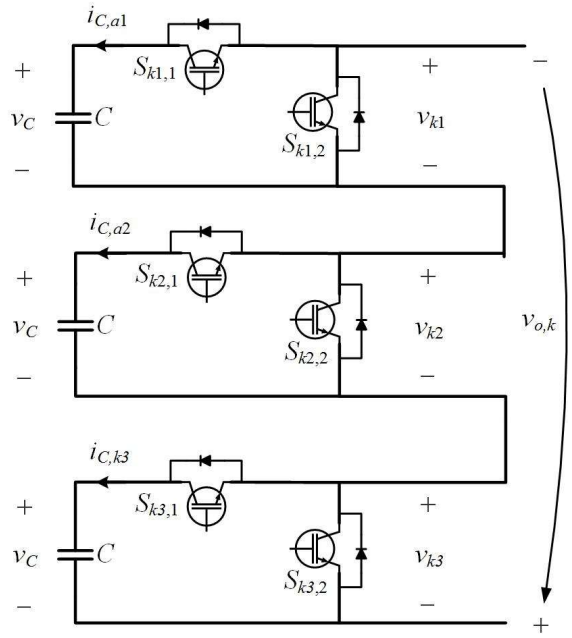

Fig. 3.2: The circuit diagram of one leg in the proposed converter when $m = 3$

Table 3.2: The switch states of the proposed converter when $m = 3$

$S_{k1,1}$	$S_{k2,1}$	$S_{k3,1}$	$S_{k1,2}$	$S_{k2,2}$	$S_{k3,2}$	$\lvert v_{o,k}\rvert$
0	0	0	1	1	1	0
0	0	1	1	1	0	v_c
0	1	0	1	0	1	v_c
1	0	0	0	1	1	v_c
0	1	1	1	0	0	$2v_c$
1	0	1	0	1	0	$2v_c$
1	1	0	0	0	1	$2v_c$
1	1	1	0	0	0	$3v_c$

3.2 Mathematical Model

Fig. 3.3 shows the equivalent model of the converter. In the proposed topology, the neutral point of the converter and the neutral point of the grid are completely separated. The converter legs must be balanced in order to cancel the DC voltage that appears across each converter leg, and

consequently running the converter as a balanced three-phase AC source. According to Kirchhoff's voltage law, the line-to-line voltages at the output terminals of the proposed converter, as depicted in the equivalent model, are given by:

$$\begin{aligned} v_{o,a}-v_{o,b} &= \left(v_a-\frac{mv_C}{2}+Ri_a+L\frac{di_a}{dt}\right)-\left(v_b-\frac{mv_C}{2}+Ri_b+L\frac{di_b}{dt}\right) \\ &= v_{ab}+R\left(i_a-i_b\right)+L\frac{d}{dt}\left(i_a-i_b\right) \\ v_{o,b}-v_{o,c} &= v_{bc}+R\left(i_b-i_c\right)+L\frac{d}{dt}\left(i_b-i_c\right) \\ v_{o,c}-v_{o,a} &= v_{ca}+R\left(i_c-i_a\right)+L\frac{d}{dt}\left(i_c-i_a\right) \end{aligned} \tag{3.4}$$

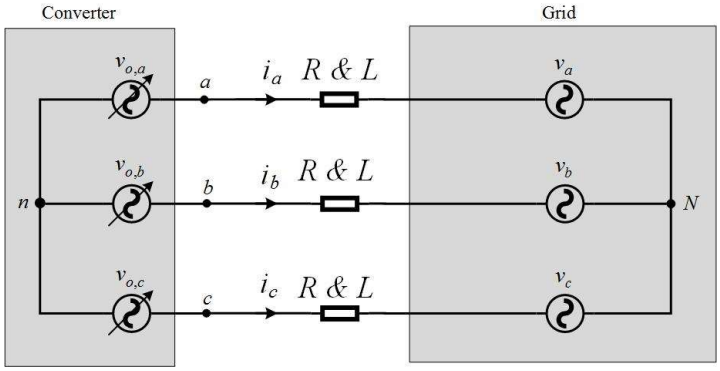

Fig. 3.3: The equivalent model of the proposed converter connected to the grid

The converter's phase *k* voltage can be mathematically modelled as:

$$\begin{aligned} v_{C,kj} &= \frac{1}{C}\int i_{C,kj}dt = \frac{1}{C}\int d_{s,kj}i_k dt \\ v_{o,k} &= -\sum_{j=1}^{m} d_{s,kj}v_{C,kj} = -\frac{1}{C}\sum_{j=1}^{m}\left(d_{s,kj}\left(\int d_{s,kj}i_k dt\right)\right) \end{aligned} \tag{3.5}$$

The proposed converter is modulated using a Carrier Disposition-Sinusoidal Pulse Width Modulation (CD-SPWM) technique with third harmonic injection. Fig. 3.4 illustrates the CD-SPWM modulation scheme, where a third-harmonic component is injected to the reference sinusoidal waves to increase the maximum peak value of the output phase voltage without losing

pulses within each cycle.

The normalized modulating waves, M_k^*, are given by:

$$M_k^* = M\sin\left(\beta+\chi_k\right)+\frac{1}{6}M\sin\left(3\beta\right);\quad \beta=\omega t+\phi;\quad \chi_k=\begin{cases}0 & k=a\\ +2\pi/3 & k=b\\ -2\pi/3 & k=c\end{cases} \tag{3.6}$$

where ω is the electric radian frequency of the modulating waves, ϕ is the phase angle of the modulating wave, and M is the modulation index of the converter, which is given by [17]:

$$M=\frac{2V_m}{mv_C};\quad 0\le M\le\frac{2}{\sqrt{3}} \tag{3.7}$$

where V_m is the peak value of the output phase voltage with respect to the grid neutral point.

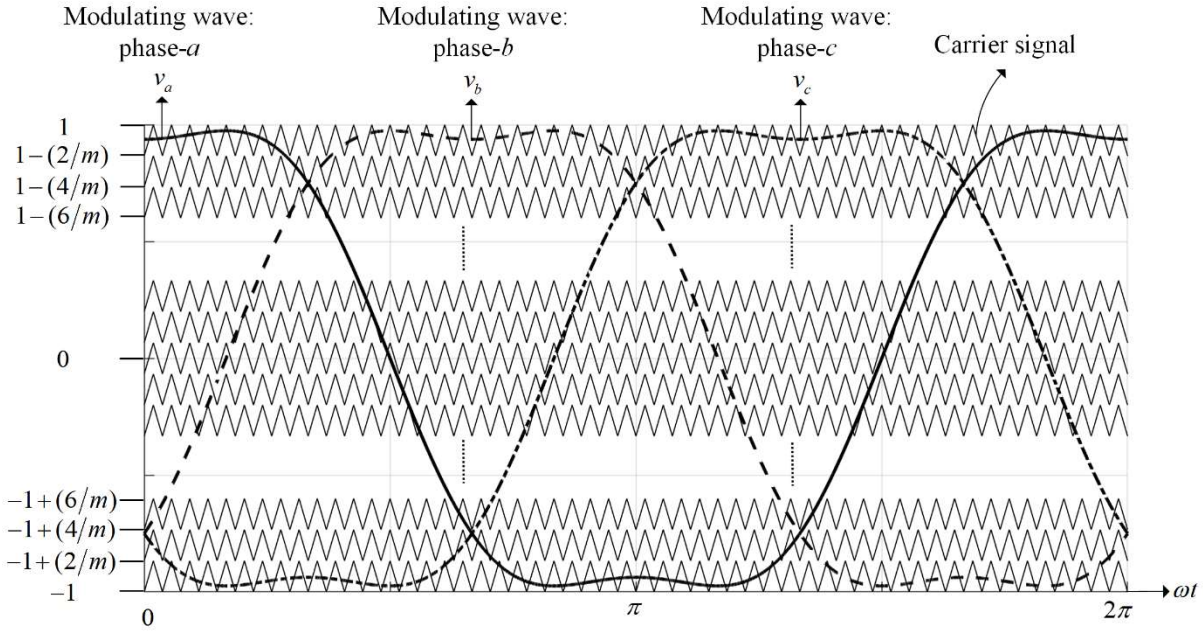

Fig. 3.4: CD-THIPWM scheme with 3rd harmonic injection

Chapter 4

Control System

The control system of the proposed converter shown in Fig. 3.1, includes three parts: converter controller, grid synchronization, and capacitor voltage-balancing controller. The main objective of the converter control is to properly feed the suitable reactive power to the grid. The grid synchronization technique is based on a Phase-Locked Loop (PLL) and it is necessary to estimate the actual phase angle of the grid. The function of the capacitor voltage-balancing controller is to balance all capacitors in each converter leg in terms of their voltages.

4.1 Converter's Control System

The control system of the converter consists of two loops: Inner control loop and outer control loop. The function of the inner loop is to control the converter's output current. The inner loop can be controlled using Direct and Quadrature (DQ) current controller. The outer control loop can be a DC-link voltage control or a power control loop, which generates the inner current references to compensate the power losses within the internal resistors of the buffer inductors.

4.1.1 Inner Control Loop

Fig. 4.1 shows the schematic of the proposed converter for grid-connected system, where an L-filter is adopted with L being the filter inductance and R being the internal resistance and $v_{o,abc}$ is the vector of the converter output voltages.

Note: This controller is derived and modelled using the same controlled used for the grid-connected Photovoltaic system [19].

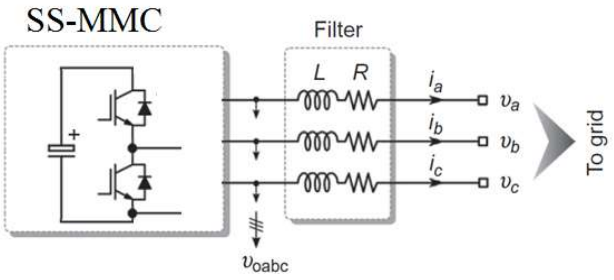

Fig. 4.1: The schematic of the proposed converter for grid-connected system

Assuming that the inverter output currents are given by:

$$\begin{aligned} i_a &= I_m \cos\left(\omega t + \varphi_i\right) \\ i_b &= I_m \cos\left(\omega t + \varphi_i - 2\pi/3\right) \\ i_c &= I_m \cos\left(\omega t + \varphi_i + 2\pi/3\right) \end{aligned} \tag{4.1}$$

where I_m is the peak value of the converter's output current and φ_i is the phase angle of the current, the Clarke transformation is used to generate an orthogonal virtual system:

$$x_{\alpha\beta} = x_\alpha + jx_\beta = \frac{2}{3}\left(x_a + x_b e^{j\frac{2\pi}{3}} + x_c e^{-j\frac{2\pi}{3}} \right) \tag{4.2}$$

The currents, i_α and i_β, are represented in stationary reference frame using Clarke transformation as:

$$i_{\alpha\beta} = i_\alpha + ji_\beta = \frac{2}{3}\left(i_a + i_b e^{j\frac{2\pi}{3}} + i_c e^{-j\frac{2\pi}{3}} \right) = I_m e^{j(\omega t + \varphi_i)} \tag{4.3}$$

The currents, i_α and i_β, are AC variables and can be converted to DC quantities in the synchronous rotating dq-reference frame using a Park transformation as:

$$i_{dq} = i_{\alpha\beta} e^{-j\theta} = i_d + ji_q \tag{4.4}$$

where $\theta = \omega t + \varphi_v$ and ω is the grid frequency. It should be noted that, the Park transformation enables the use of PI controllers. By applying KVL in stationary reference frame, we get

$$
\begin{aligned}
&v_{o,a} = Ri_a + L\frac{di_a}{dt} + v_a \\
&v_{o,b} = Ri_b + L\frac{di_b}{dt} + v_b \Rightarrow \begin{cases} v_{o,\alpha} = Ri_\alpha + L\dfrac{di_\alpha}{dt} + v_\alpha \\ v_{o,\beta} = Ri_\beta + L\dfrac{di_\beta}{dt} + v_\beta \end{cases} \\
&v_{o,c} = Ri_c + L\frac{di_c}{dt} + v_c \\
&\Rightarrow v_{o,\alpha\beta} = Ri_{\alpha\beta} + L\frac{di_{\alpha\beta}}{dt} + v_{\alpha\beta}
\end{aligned}
\tag{4.5}
$$

The last equation can be transferred to the rotating reference frame as:

$$
\begin{aligned}
&v_{o,dq}e^{j\theta} = Ri_{dq}e^{j\theta} + L\frac{d\left(i_{dq}e^{j\theta}\right)}{dt} + v_{dq}e^{j\theta}; \qquad \theta=\omega t+\varphi_v \\
&v_{dq}e^{j\theta} = Ri_{dq}e^{j\theta} + Le^{j\theta}\frac{di_{dq}}{dt} + j\omega Li_{dq}e^{j\theta} + v_{dq}e^{j\theta} \\
&v_{o,dq} = Ri_{dq} + L\frac{di_{dq}}{dt} + j\omega Li_{dq}
\end{aligned}
\tag{4.6}
$$

The final KVL equation in *dq*-domain is given by:

$$
v_{o,dq} = Ri_{dq} + L\frac{di_{dq}}{dt} + j\omega Li_{dq} \Rightarrow \begin{cases} v_{o,d} = Ri_d + L\dfrac{di_d}{dt} - \omega Li_q + v_d \\ v_{o,q} = Ri_q + L\dfrac{di_q}{dt} + \omega Li_d + v_q \end{cases}
\tag{4.7}
$$

Assuming that the grid voltages are given by:

$$
\begin{aligned}
v_a &= V_m\cos(\theta); \qquad \theta=\omega t+\varphi_v \\
v_b &= V_m\cos(\theta-2\pi/3) \\
v_c &= V_m\cos(\theta+2\pi/3)
\end{aligned}
\tag{4.8}
$$

The grid voltages, v_α and v_β, are represented in stationary reference frame using Clarke transformation as:

$$
v_{\alpha\beta} = v_\alpha + jv_\beta = \frac{2}{3}\left(v_a + v_b e^{j\frac{2\pi}{3}} + v_c e^{-j\frac{2\pi}{3}}\right) = V_m e^{j\theta}
\tag{4.9}
$$

The voltages, v_α and v_β, are represented in the rotating reference frame as (Park transformation):

$$v_{dq} = v_d + jv_q = v_{\alpha\beta} e^{-j\theta} = V_m; \quad v_d = V_m \ \& \ v_q = 0 \tag{4.10}$$

The final KVL equation in *dq*-domain is given by:

$$\begin{aligned} v_{o,d} &= \underbrace{Ri_d + L\frac{di_d}{dt}}_{u_d} - \omega L i_q + v_d \\ v_{o,q} &= \underbrace{Ri_q + L\frac{di_q}{dt}}_{u_q} + \omega L i_d \end{aligned} \tag{4.11}$$

The implementation of DQ current controller without the DC voltage regulator is shown in Fig. 4.2. The active and reactive power can be easily calculated using the *dq*-quantities of the three-phase voltages and currents as follows:

$$P = 1.5 v_d i_d; \quad Q = -1.5 v_d i_q \tag{4.12}$$

Therefore, the references values, i_d^* and i_q^*, are estimates using the last equation where i_d^* is set to be zero and i_q^* is directly proportional to the reactive power absorbed by the load to guarantee that the grid feeds the load at unity power factor.

$$i_d^* = 0; \quad i_q^* = -Q_{\text{load}} / (1.5 v_d) \tag{4.13}$$

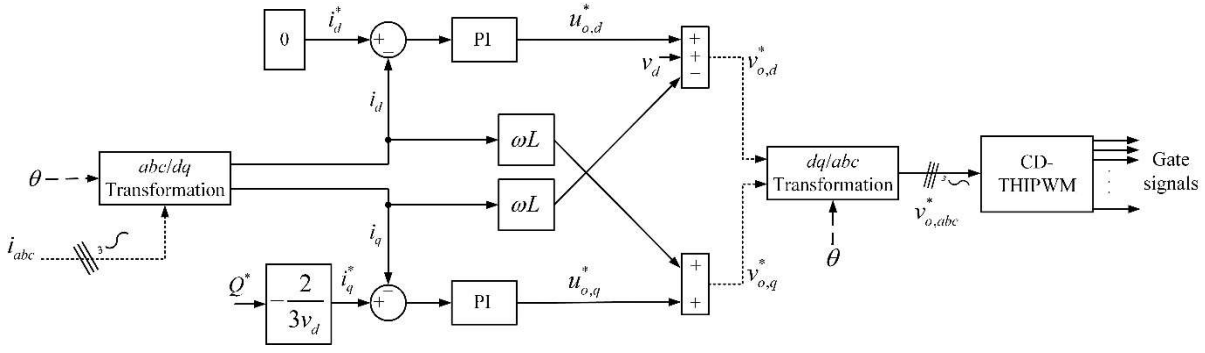

Fig. 4.2: The implementation of DQ current controller without inner DC voltage regulator

The mathematical model of the current control system in both *t* and *s*-domains is given by:

$$u_d = Ri_d + L\left(di_d/dt\right), \quad u_q = Ri_q + L\left(di_q/dt\right)$$
$$U_d = \left(R + sL\right)I_d; \quad U_q = \left(R + sL\right)I_q \tag{4.14}$$

Therefore, the direct transfer function of the current controller is given by:

$$G = \frac{I_d}{U_d} = \frac{I_q}{U_q} = \frac{1}{R + sL} = \frac{1}{R}\left(\frac{1}{1 + \tau_f s}\right); \quad \tau_f = \frac{L}{R} \tag{4.15}$$

where τ_f is the plant time constant. Fig. 4.3 shows the closed-loop current control system in the synchronous rotating reference. Considering the PI current controller as:

$$G_c = K_1 + \frac{K_2}{s} = K_1\left(\frac{1 + \tau_i s}{\tau_i s}\right); \quad \tau_i = \frac{K_1}{K_2} \tag{4.16}$$

where τ_i is the integrator time constant. The transfer function of the elapsed delay, including the PWM and computation time in the control system is given by:

$$G_d = \frac{1}{1 + \tau_d s} \tag{4.17}$$

where τ_d being the delay time constant. The open loop transfer function is given by:

$$G_{OL,cc} = G_c G G_d = \frac{K_1}{R}\left(\frac{1 + \tau_i s}{\tau_i s}\right)\left(\frac{1}{1 + \tau_d s}\right)\left(\frac{1}{1 + \tau_f s}\right) \tag{4.18}$$

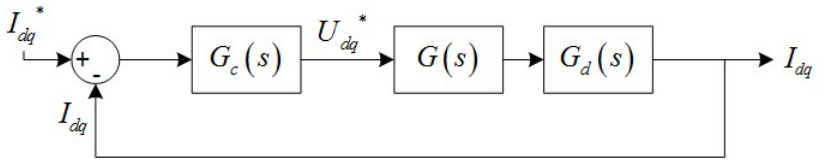

Fig. 4.3: The closed-loop current control system

Clearly, the model is a third-order system and it can be simplified by designing the time constant of the PI controller as the plant time constant (i.e., $\tau_i = \tau_f$), the model is then simplified as:

$$G_{OL,cc} = \frac{K_1}{Ls\left(1+\tau_d s\right)} \tag{4.19}$$

The closed loop transfer function is given by:

$$T_{cc} = \frac{G_{OL,cc}}{1+G_{OL,cc}} = \frac{\left(K_1/L\tau_d\right)}{s^2+\left(1/\tau_d\right)s+\left(K_1/L\tau_d\right)} \tag{4.20}$$

which becomes a typical second-order system with:

$$\begin{aligned} T_{cc} &= \frac{{\omega_n}^2}{s^2+\left(2\zeta\omega_n\right)s+{\omega_n}^2} = \frac{\left(K_1/L\tau_d\right)}{s^2+\left(1/\tau_d\right)s+\left(K_1/L\tau_d\right)} \\ \frac{K_1}{L\tau_d} &= {\omega_n}^2, \qquad 2\zeta\omega_n = \frac{1}{\tau_d} \end{aligned} \tag{4.21}$$

In practice, $\zeta = 0.707$ results in an optimally damped system with an overshoot of approximately 5%. Therefore, the proportional and integral constants can be obtained as:

$$\begin{aligned} T_{cc} &= \frac{{\omega_n}^2}{s^2+\left(2\zeta\omega_n\right)s+{\omega_n}^2} = \frac{\left(K_1/L\tau_d\right)}{s^2+\left(1/\tau_d\right)s+\left(K_1/L\tau_d\right)} \\ \frac{K_1}{L\tau_d} &= {\omega_n}^2, \qquad 2\zeta\omega_n = \frac{1}{\tau_d} \end{aligned} \tag{4.22}$$

4.1.2 Outer Control Loop

The function of the outer control loop is to regulate the DC voltage across the embedded capacitors and compensate the power losses within the internal resistors of the buffer inductors. This controller will generate of the d-axis component of the converter's output current.

The active power absorbed by the proposed converter is controlled through the regulation of the capacitor voltages within SMs. These capacitor voltages are maintained constant and controlled at a desired voltage, which is the average capacitive voltage, $v_{C,avg}$, for all SMs. The average capacitor voltage of all SMs is calculated as:

$$v_{C,avg} = \frac{1}{3m}\left(\sum_{j=1}^{m} v_{C,aj} + \sum_{j=1}^{m} v_{C,bj} + \sum_{j=1}^{m} v_{C,cj}\right) \tag{4.23}$$

It should be pointed out that, to ensure a proper voltage regulation and avoid over modulation, the average capacitive voltage has to be at least higher than the peak line voltage divided over the number of SMs:

$$v_C^* > \frac{\sqrt{3}V_m}{m} \tag{4.24}$$

Neglecting the power losses within the SMs and the power losses absorbed by the internal resistances of the buffer inductors, the power used to charge the capacitors and the input active power should be equal. Hence, it yields [19]:

$$\begin{cases} P_{dc} = 3mv_{C,avg} C\dfrac{dv_{C,avg}}{dt} \\ P_{ac} = \dfrac{3}{2} v_d i_d \end{cases} \xrightarrow{P_{dc} \approx P_{ac}} (3mC) v_{C,avg} \frac{dv_{C,avg}}{dt} = \frac{3}{2} v_d i_d \tag{4.25}$$

where P_{dc} is the DC power routed to the converter and P_{ac} is the active power at the converter's AC side.

The last equation can help to design the outer DC voltage regulator using a traditional PI controller to generate of the reference d-axis component of the converter's output current. Since this equation is non-linear, it is hard to derive the transfer function of the DC voltage regulator. Therefore, the gains of the PI controller, $K_{1,dc}$ and $K_{2,dc}$ should be selected using a tuning method.

4.2 Grid Synchronization

It can be seen from the DQ current controller that the grid-voltage phase, θ, is essential to the converter control. The phase can be extracted by means of phase-locked loop (PLL) systems, and

this process is called grid synchronization. The basic structure of the grid synchronization system in grid-connected applications is shown in Fig. 4.4.

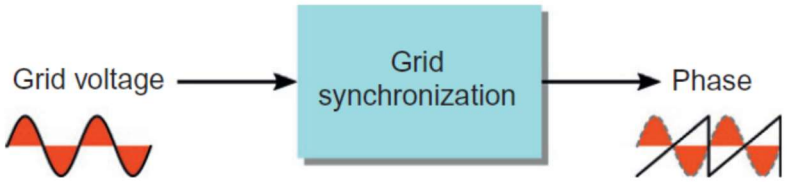

Fig. 4.4: The basic structure of the grid synchronization system

Assume that the grid voltages are given by:

$$\begin{aligned} v_a &= V_m \cos(\theta); \quad \theta = \int \omega\, dt \approx \omega t + \varphi_v \\ v_b &= V_m \cos(\theta - 2\pi/3) \\ v_c &= V_m \cos(\theta + 2\pi/3) \end{aligned} \tag{4.26}$$

The voltages, v_α and v_β, are represented in stationary reference frame using Clarke transformation as:

$$v_{\alpha\beta} = v_\alpha + jv_\beta = \frac{2}{3}\left(v_a + v_b e^{j\frac{2\pi}{3}} + v_c e^{-j\frac{2\pi}{3}} \right) = V_m e^{j\theta} \tag{4.27}$$

The voltages, v_α and v_β, are represented in rotating reference frame as (Park transformation) [12], [20]:

$$\begin{aligned} v_{dq} &= v_d + jv_q = v_{\alpha\beta} e^{-j\theta_{est}} = \left(V_m e^{j\theta} \right) e^{-j\theta_{est}} = V_m e^{j(\theta - \theta_{est})} \\ v_d &= V_m \cos(\theta - \theta_{est}) \approx V_m \\ v_q &= V_m \sin(\theta - \theta_{est}) \approx V_m e; \quad e = \theta - \theta_{est} \end{aligned} \tag{4.28}$$

The mathematical model of the grid frequency in t and s-domains is given by:

$$\omega = \frac{d\theta}{dt} \xrightarrow{Laplace} \Omega = s\Theta \tag{4.29}$$

Therefore, the direct transfer function of the PLL is:

$$G = \frac{\Theta}{\Omega} = \frac{1}{s} \tag{4.30}$$

The implementation of three-phase PLL to estimate the phase angle of the grid voltage is shown in Fig. 4.5 while the closed loop control system of the PLL is shown in Fig. 4.6. The closed loop transfer function is derived as follows [12], [20]:

$$T_{PLL} = \frac{\Theta_{est}}{\Theta} = \frac{GG_c}{1+GG_c} = \frac{\left(\frac{K_1 s + K_2}{s^2}\right)}{1+\left(\frac{K_1 s + K_2}{s^2}\right)} \tag{4.31}$$

$$T_{PLL} = \frac{K_1 s + K_2}{s^2 + K_1 s + K_2}$$

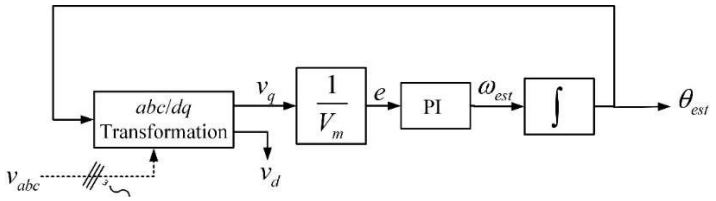

Fig. 4.5: The Implementation of three-phase PLL

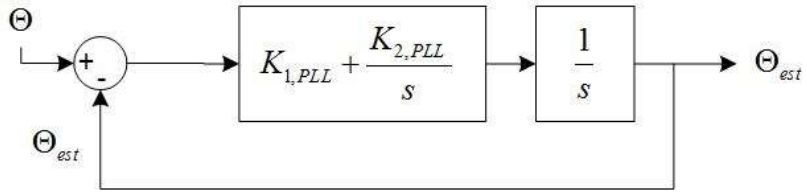

Fig. 4.6: The closed loop control system of the PLL

The closed loop transfer function can be further represented as [12], [20]:

$$\begin{aligned} T_{PLL} &= \frac{\left(1+\left(K_{1,PLL}/K_{2,PLL}\right)s\right)K_{2,PLL}}{s^2+K_{1,PLL}s+K_{2,PLL}} \\ &\approx \frac{K_{2,PLL}}{s^2+K_{1,PLL}s+K_{2,PLL}} = \frac{\omega_n{}^2}{s^2+\left(2\zeta\omega_n\right)s+\omega_n{}^2} \\ K_{1,PLL} &= 2\zeta\omega_n \\ K_{2,PLL} &= \omega_n{}^2 \end{aligned} \tag{4.32}$$

The controller gains, $K_{1,PLL}$ and $K_{2,PLL}$, can be easily designed as follows K_1 and K_2:

- Determine the settling time t_s (e.g, 10 ms) and the damping ratio ζ (e.g, 0.707)
- Calculate ω_n where $\omega_n = 4/(\zeta t_s)$
- Calculate $K_{1,PLL}$ and $K_{2,PLL}$

4.3 Capacitor Voltage-Balancing Controller

The main objective of the capacitor voltage-balancing controller is to balance all capacitors in each converter leg in terms of their voltages. Fig. 4.7 shows the flowchart of the capacitor voltage balancing strategy for leg *k*.

Using this method, the balancing of capacitor voltages is guaranteed within the leg and all capacitors will have the same voltage, which is equal to the average capacitive voltage of that leg. The procedure to balance the capacitors in terms of their voltages within each leg can be summarized as follows:

1. Measure all capacitor voltages
2. Sort the capacitors in a descending order
3. Calculate the number of active SMs

4. Measure the leg current i_k
5. Switch on the capacitors with the lowest voltages if i_k is charging the capacitors or switch on the capacitors with the highest voltages if i_k is discharging the capacitors.

Assume that $m = 4$ and the capacitor voltages are $v_{C,a1} = 70$ V, $v_{C,a2} = 80$ V, $v_{C,a3} = 50$ V, and $v_{C,a4} = 90$ V:

- If the number of active SMs is 2 and i_a is charging the capacitors ($i_a > 0$), then the gate signals will be:

$$\begin{bmatrix} d_{s,a1} & d_{s,a2} & d_{s,a3} & d_{s,a4} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 \end{bmatrix} \tag{4.33}$$

- If the number of active SMs is 2 and i_a is discharging the capacitors ($i_a < 0$), then the gate signals will be:

$$\begin{bmatrix} d_{s,a1} & d_{s,a2} & d_{s,a3} & d_{s,a4} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 1 \end{bmatrix} \tag{4.34}$$

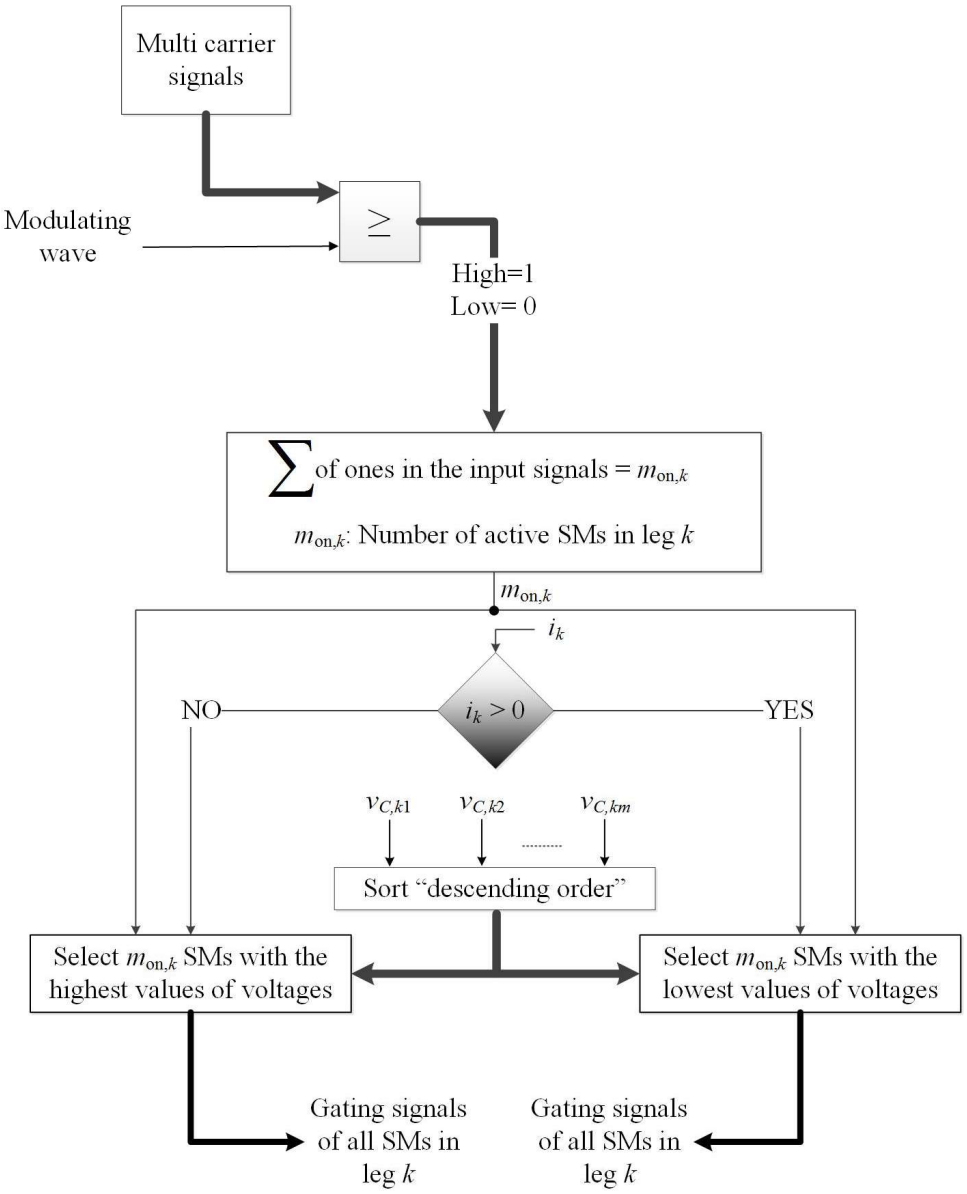

Fig. 4.7: The capacitor voltage balancing control strategy of leg k

Chapter 5

Simulation Results

To demonstrate the main characteristics of the proposed converter as a STATCOM, the proposed system has been simulated using Matlab/Simulink. The converter has been simulated under static load conditions with DQ current controller and PLL algorithm.

5.1 DQ Current Controller with Grid Synchronization

In this section, the behaviour of the proposed converter, when it is connected to the grid with a current controller and a PLL controller, has been tested by means of numerical simulations. A three-phase, 400 V, and 50 Hz grid is connected to the AC terminals of the converter. The filter's line resistance and inductance are assumed to be 150 mΩ and 1 mH, respectively. A three-phase, 20 kW load is connected to the grid with a 0.7 power factor (lagging). The converter is modulated implementing the THI-SPWM at a switching frequency of 4.05 kHz.

Fig. 5.1 shows the simulated model of the three-phase PLL and the results in Fig. 5.2 show the responses of the PLL controller when its settling time is chosen to be 40 ms, where the damping ratio of the controller is set to be 0.707. Table 5.1 summarizes the control gains of the PLL that are used in the simulation. It is clear that, the PLL controller is able to estimate angular position of the grid where the error converges to zero in the steady state.

Table 5.1: Control gains of PLL

Proportional gain	$K_{1,PLL}$	200 rad/(V.s)
Integral gain	$K_{2,PLL}$	20×10^3 rad/(V.s^2)

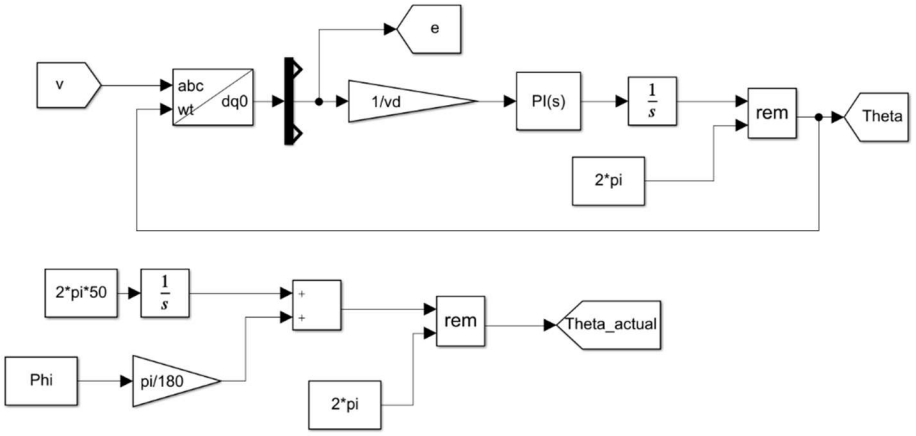

Fig. 5.1: The simulated PLL model

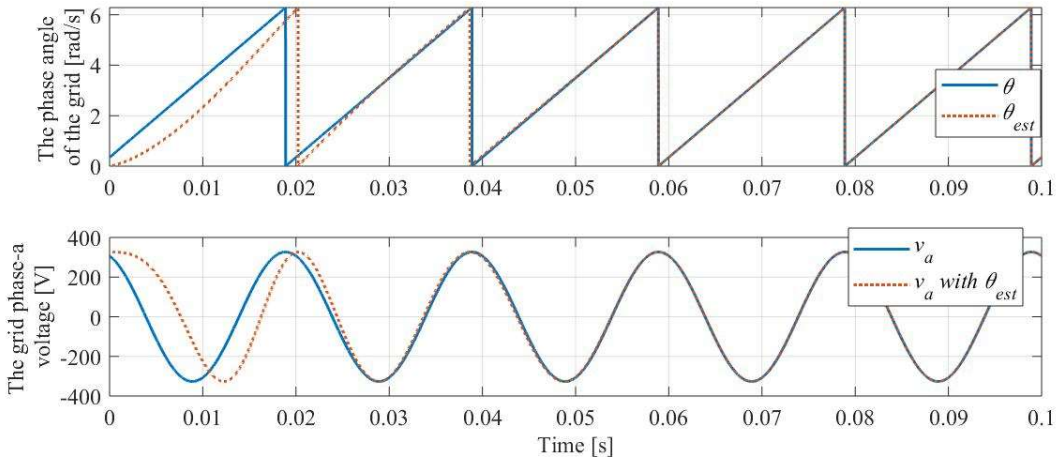

Fig. 5.2: The response of the PLL at a settling time of 40 ms

In order to study the effect of the converter levels on the THD, different numbers of SMs have been applied. The results in Fig. 5.3, Fig. 5.4, Fig. 5.5, and Fig. 5.6 show the converter's line voltages and currents all measured at *m* equals to 2, 4, 6, and 8, respectively. It is clear that, the converter produces more voltage levels for a higher number of SMs and the THD of the converter line current decreases with increasing the number of SMs within each leg as shown in Fig. 5.7.

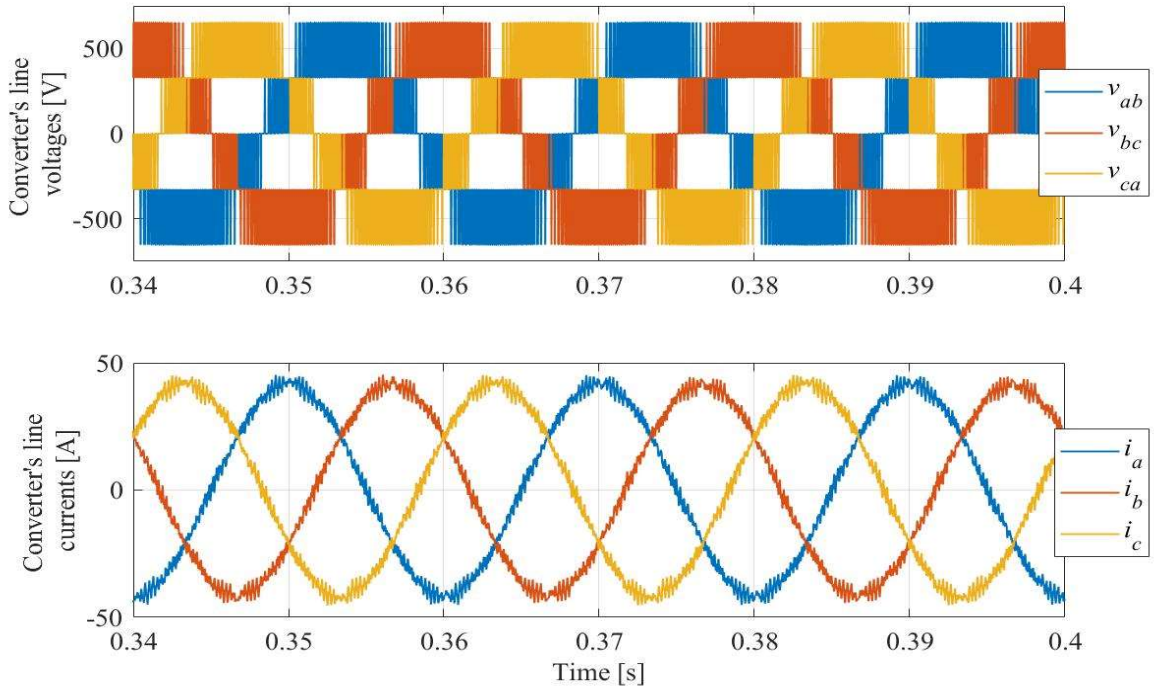

Fig. 5.3: The converter's line voltages and currents with $m = 2$

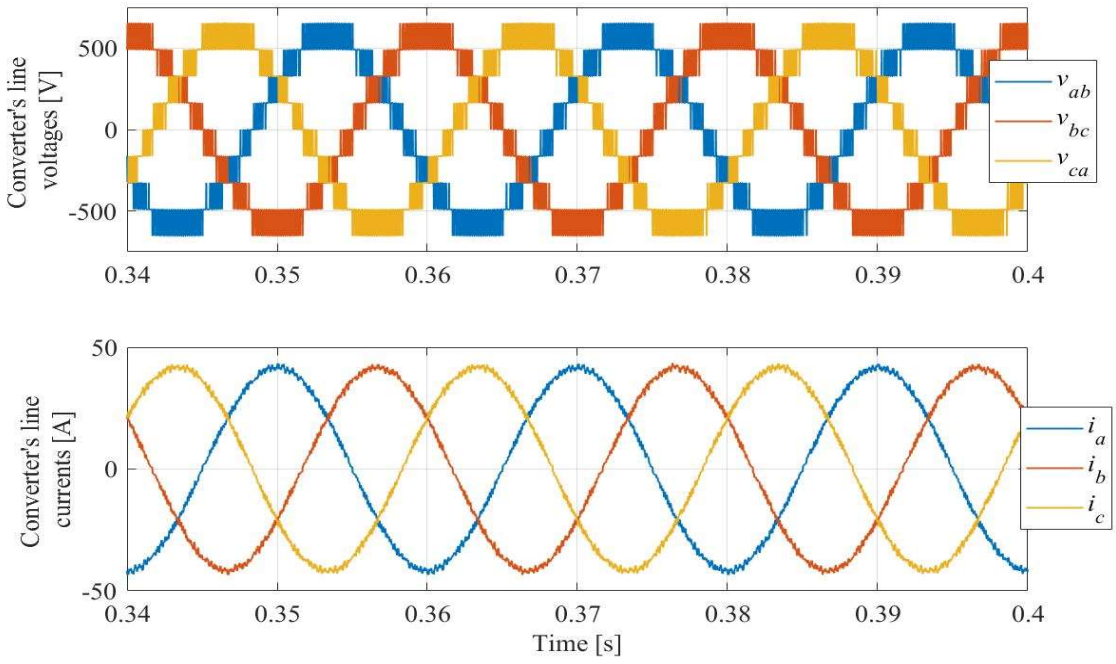

Fig. 5.4: The converter's line voltages and currents with $m = 4$

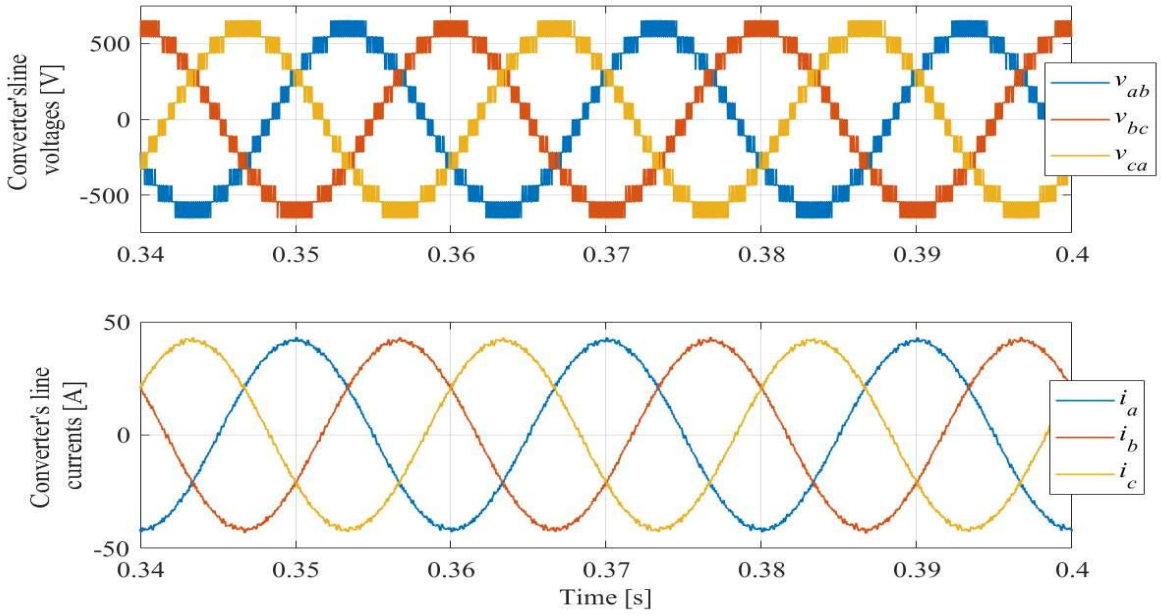

Fig. 5.5: The converter's line voltages and currents with $m = 6$

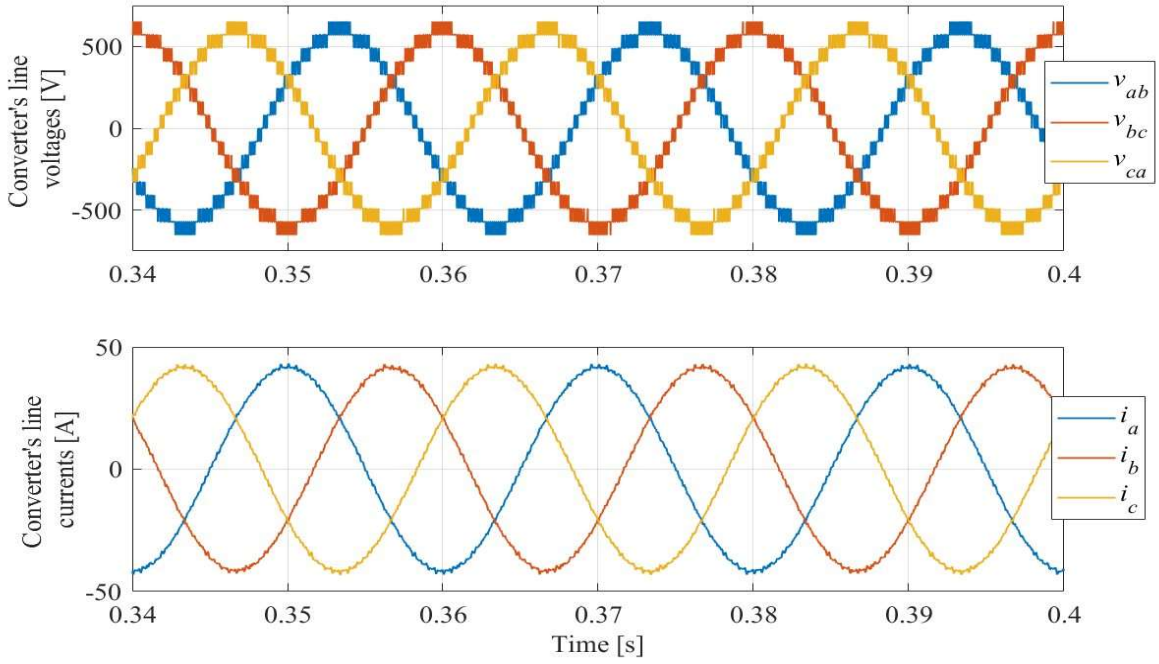

Fig. 5.6: The converter's line voltages and currents with $m = 8$

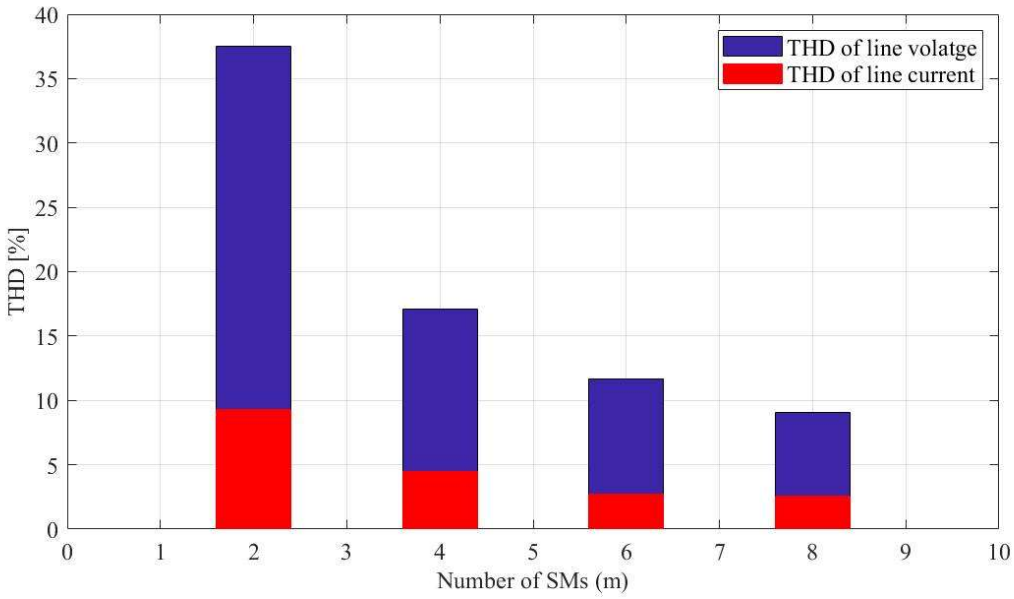

Fig. 5.7: The THD of the converter's line voltage and current versus *m*

Fig. 5.8 shows the converter line voltages and currents measured at *m* equals 8 again to show the results at the starting time of simulation. It is clear that, the converter transient current is about 10 times the steady state current. However, this current is limited in practice due to the internal resistances of switches and wires. The proposed control system needs at least one cycle to be fed by the measured reactive power and then generate the appropriate gate pulses to the switches to compensate the load reactive power.

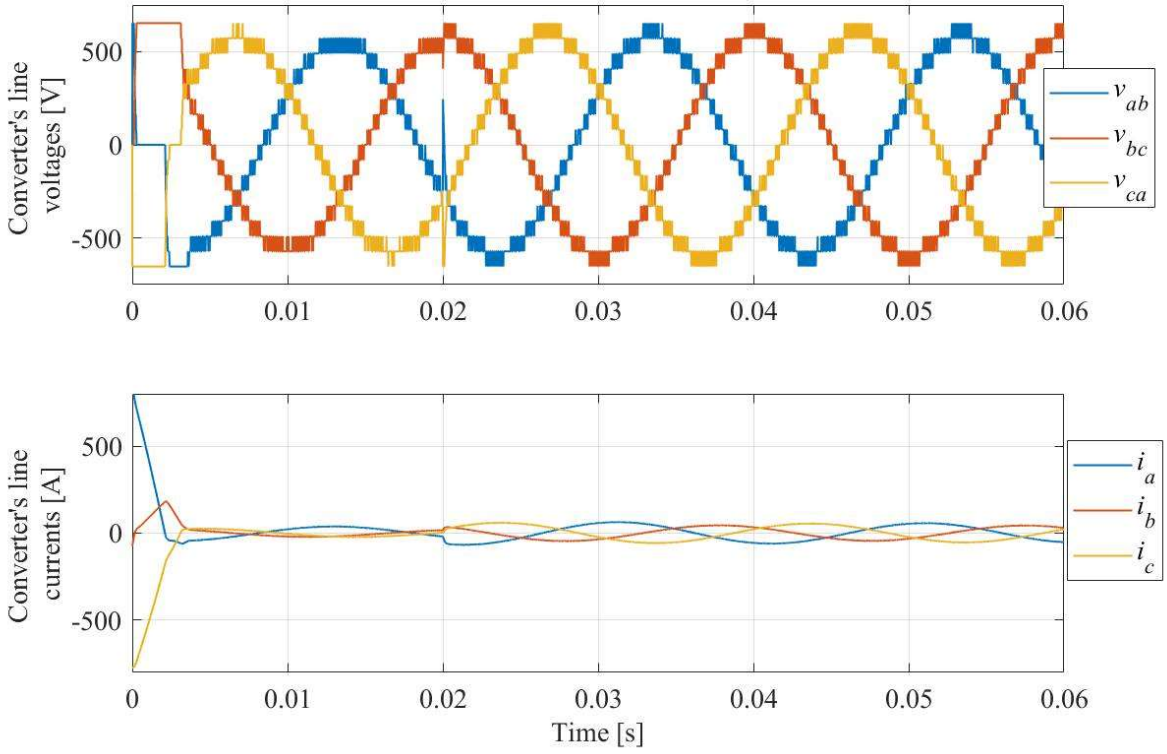

Fig. 5.8: The converter's line voltages and currents (m = 8)-the results are measured from the starting time of simulation

Fig. 5.9 shows the simulated model of the proposed converter when it is connected to the grid where each leg of the converter consists of 10 SMs, while Fig. 5.10 shows the simulated model of DQ current controller. The reference quadrature component of the converter's line currents has been set to a value, which is proportional to the reactive power absorbed by the load, while the reference direct-axis component has been set to zero to make the grid operate at a nearly unity power factor. Table 5.2 summarizes the control gains of the PLL that are used in the simulation when the delay time constant is chosen to be 1 ms and the damping ratio of the controller is set to be 0.707.

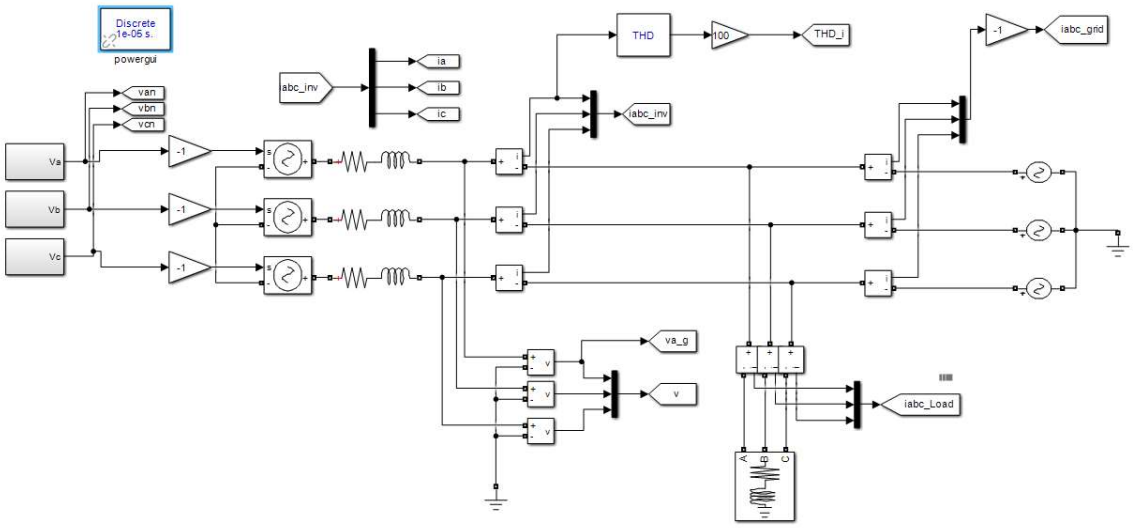

Fig. 5.9: The simulation model of the system

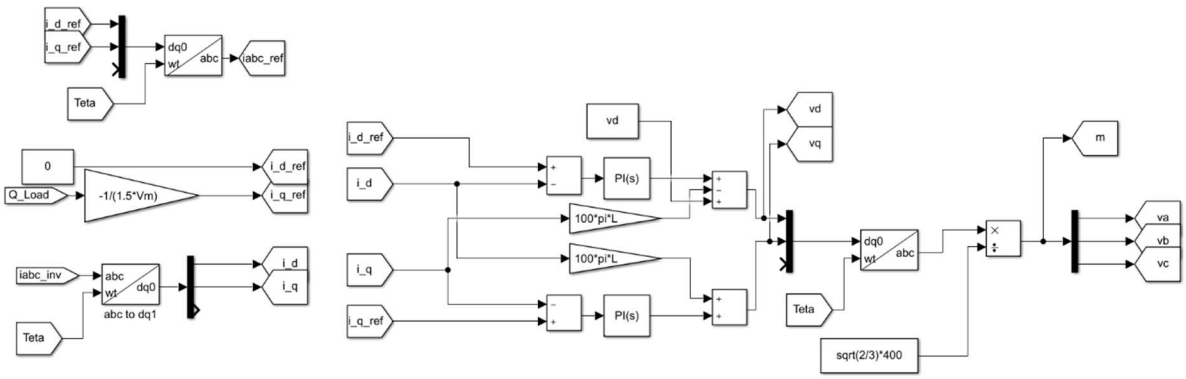

Fig. 5.10: The simulation DQ-controller model

Table 5.2: Control gains of the current controller

Proportional gain	K_1	0.5 V/A
Integral gain	K_2	75 (V.s)/A

Fig. 5.11 shows the converter's line-to-line voltages and the converter line currents. It is clear that, the converter produces a high quality line current with a THD of 1.8 %, due to the filtering

effect of the added inductance and the high number of levels.

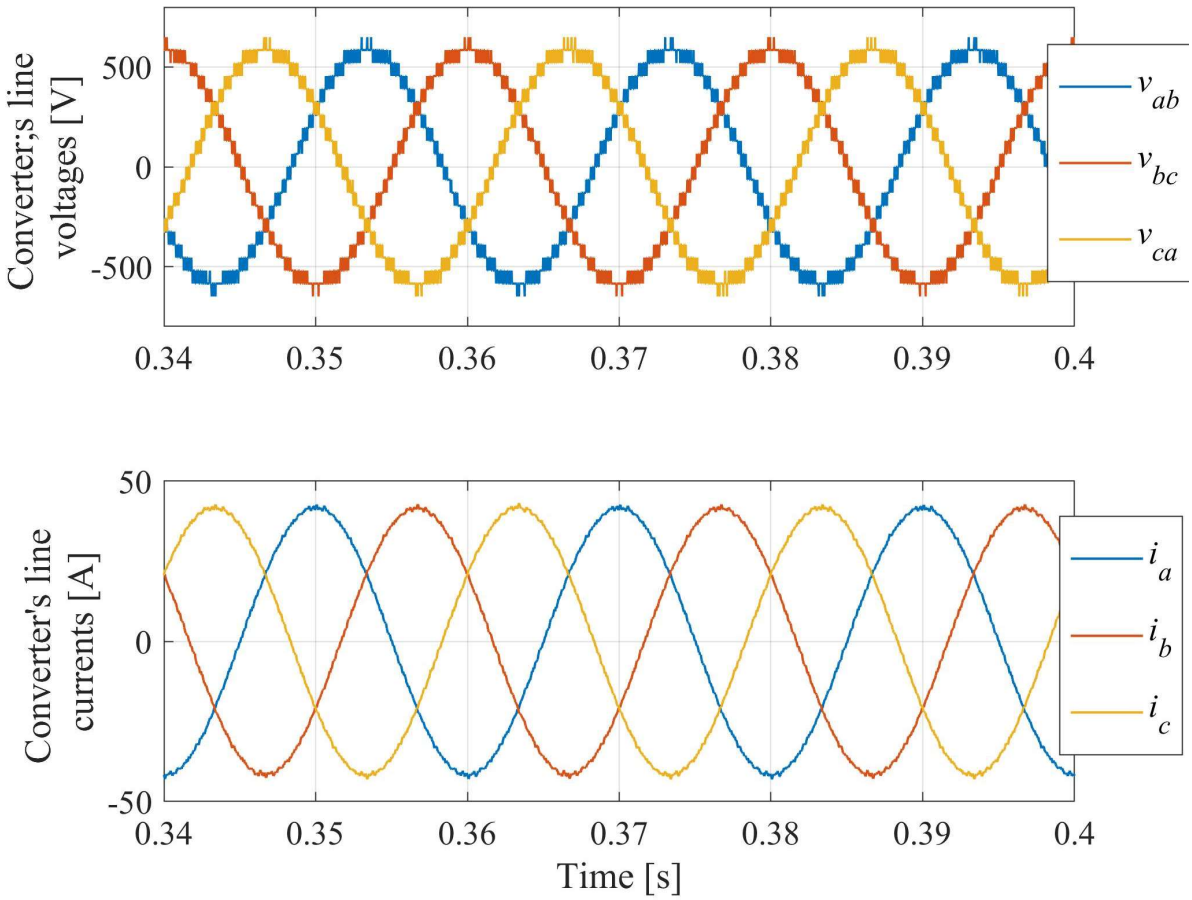

Fig. 5.11: The converter's line-to-line voltages and line currents with $m = 10$

Fig. 5.12 and Fig. 5.13 show the measured *dq*-components and *abc*-components of the converter's line currents, respectively. The results show a good capability of tracking the reference currents and these waveforms confirmed a stable operation of the proposed converter even during the transient states.

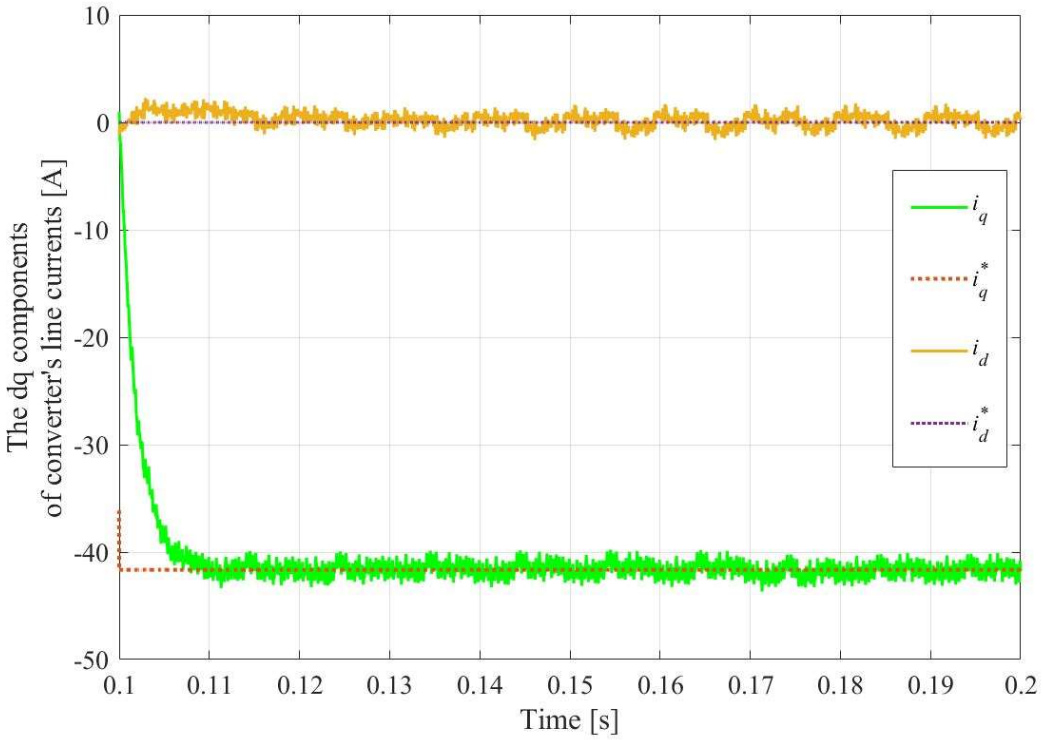

Fig. 5.12: The *dq*-components of the converter's line currents

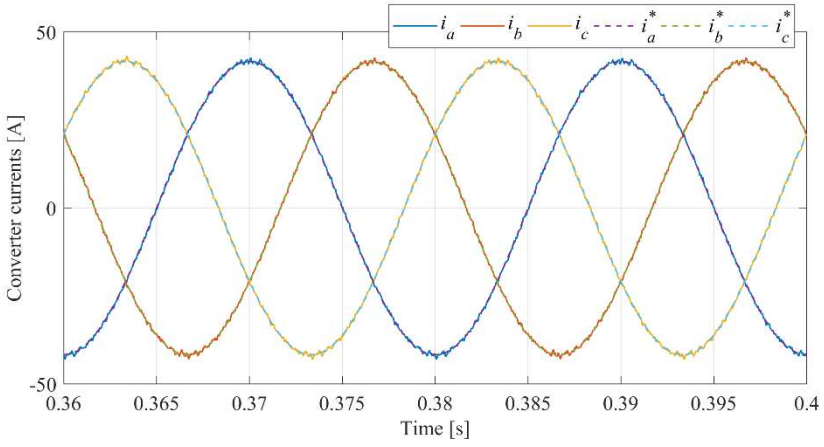

Fig. 5.13: The *abc*-components of the converter's line currents

Fig. 5.14 presents the grid's measured phase voltages and currents and Fig. 5.15 shows the load's phase voltages and currents. It is worth noting that, the grid phase currents and voltages are in

phase and the grid is able to operate at a unity power factor.

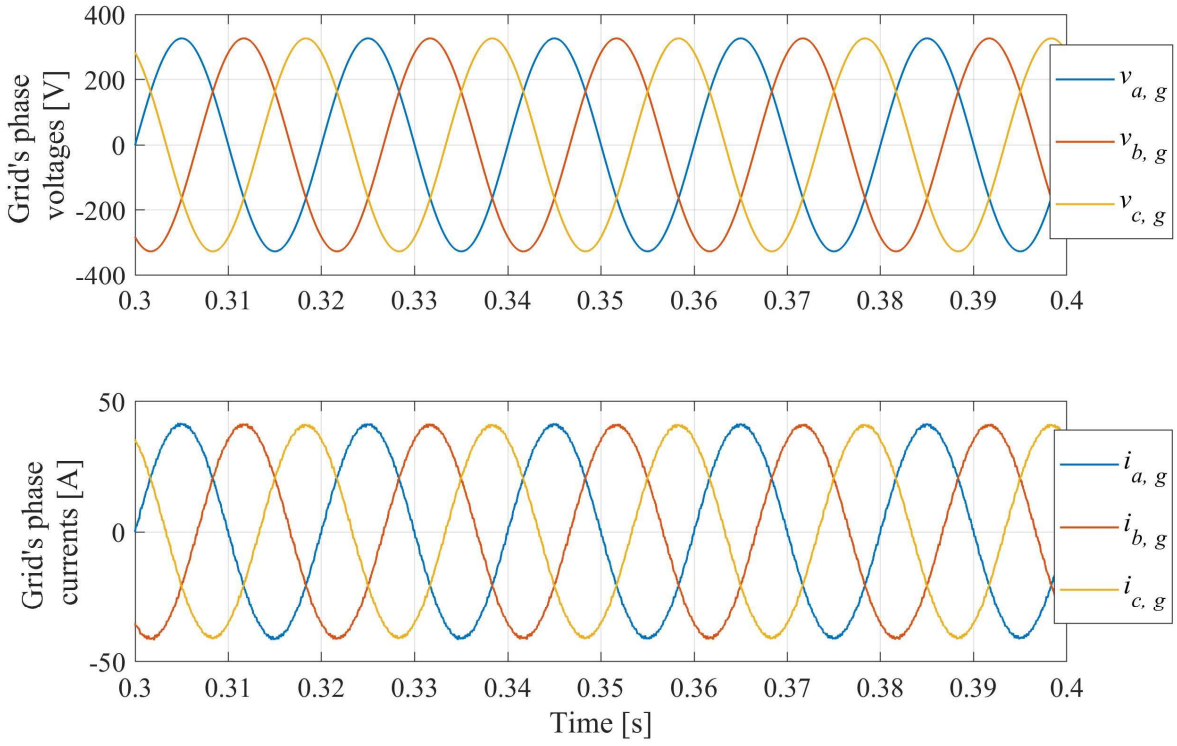

Fig. 5.14: The grid's phase voltages and currents with $m = 10$

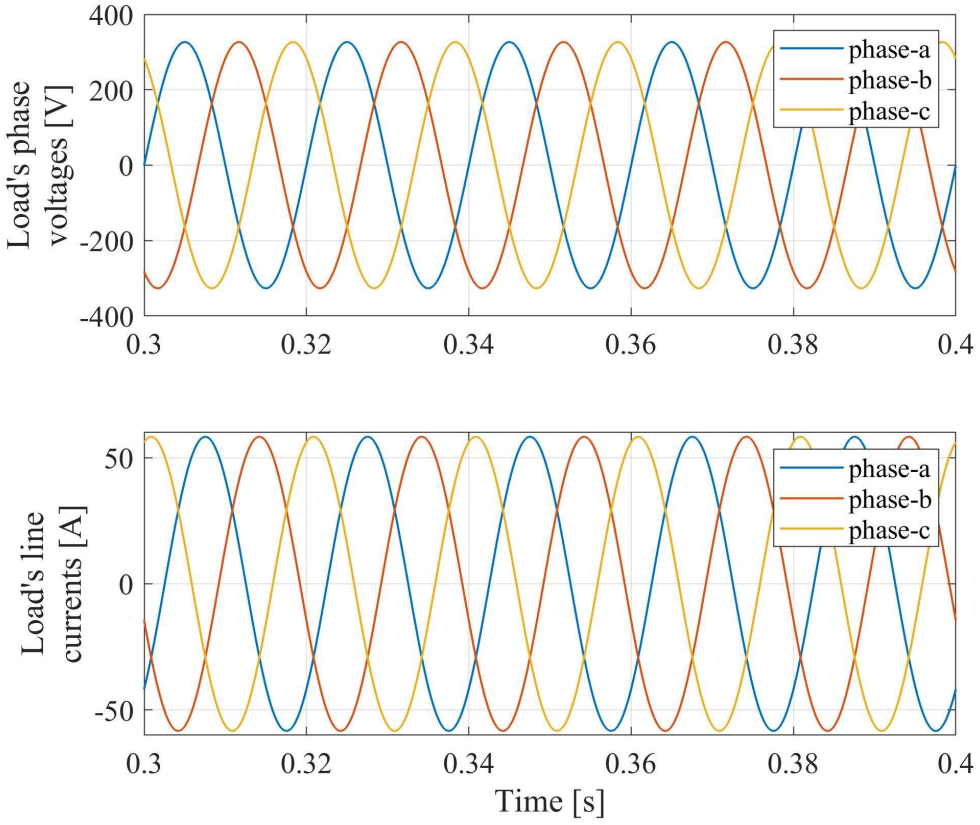

Fig. 5.15: The load's phase voltages and currents with m = 10

Fig. 5.16 shows the power generated by the grid, the power generated by the converter, and the power absorbed by the load. It can be seen from the results that, the total active power absorbed by the load (20 kW) is fed from the grid while the total reactive power absorbed by the load (20.4 kVAR) is fed from the converter. As a result, the converter is able to make the grid to operate at a unity power factor.

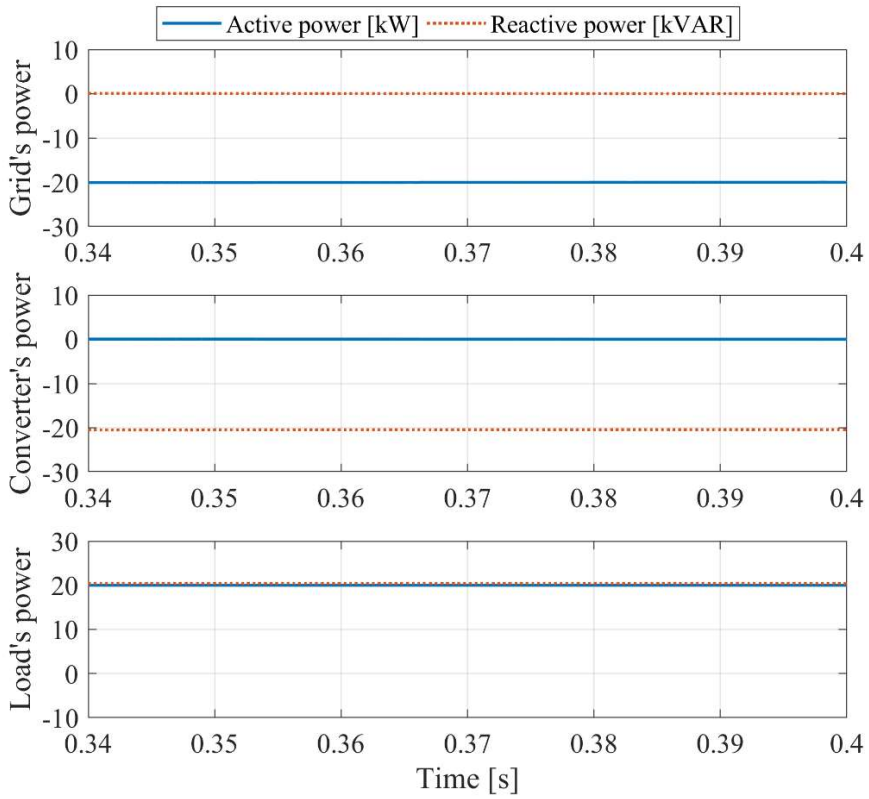

Fig. 5.16: The power generated by the grid, the power generated by the converter, and the power absorbed by the load from top to bottom, respectively

5.2 Capacitor Voltage Balancing Controller

The behaviour of the proposed STATCOM, when it is connected to a 33 kV distribution system with a current controller and capacitor voltage balancing algorithm, has been tested by means of numerical simulations. The power is transmitted to 10 MVA, 400 V loads via two feeders (20 km and 10 km) and two 33kV/400V distributed transformers. In order to verify the response of the current controller, a step change at $t = 2$ seconds in the reactive power absorbed by the two loads has been applied so that their power factor changed from 0.6 to 0.8 lagging. Fig. 5.17 shows the simulated model of the load where this load variation will allow to observe the ability of the proposed STATCOM to generate the appropriate reactive power to the distribution network.

Fig. 5.18 shows the simulated model of the system and Table 5.3 summarizes the model parameters used for simulation while Table 5.4 includes all the gains used in our design for different controllers. In order to speed-up simulation while keeping simulation fidelity, each leg of the converter has been modelled as shown in Fig. 5.19 using equation (3.15).

Table 5.3: Model Parameters

Rated reactive power	10 MVAR
Rated line voltage	33 kV
Filter inductance	75 mH
Capacitor voltage reference	1.6 kV
Capacitor capacitance	10 mF
Number of SMs/leg	35
Switching frequency	4.05 kHz
Resistance of feeder per unit length	0.215 mΩ/km
Inductance of feeder per unit length	5.4 mH/km

Table 5.4: Control gains of PLL, Current Controller, DC Voltage Regulator

PLL Proportional gain	$K_{1,\,PLL}$	200 rad/ (V.s)
PLL Integral gain	$K_{2,\,PLL}$	20000 rad/ (V.s^2)
Current Controller Proportional gain	K_1	37.5 (V/A)
Current Controller Integral gain	K_2	312.5 (V.s)/A
DC Voltage Regulator Proportional gain	$K_{1,\,dc}$	0.06 (A/V)
DC Voltage Regulator Integral gain	$K_{2,\,dc}$	5.325 (A.s)/V

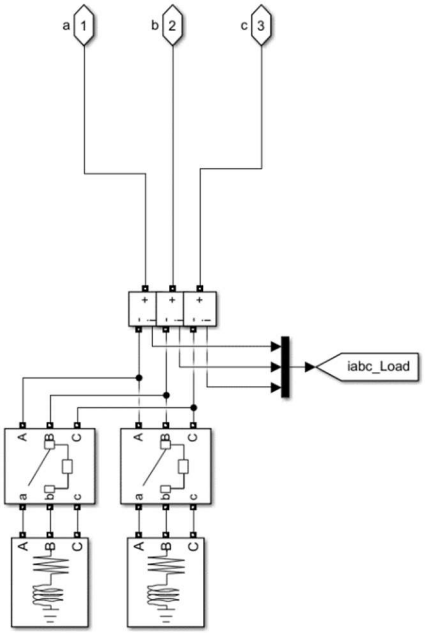

Fig. 5.17: The simulation model of the load

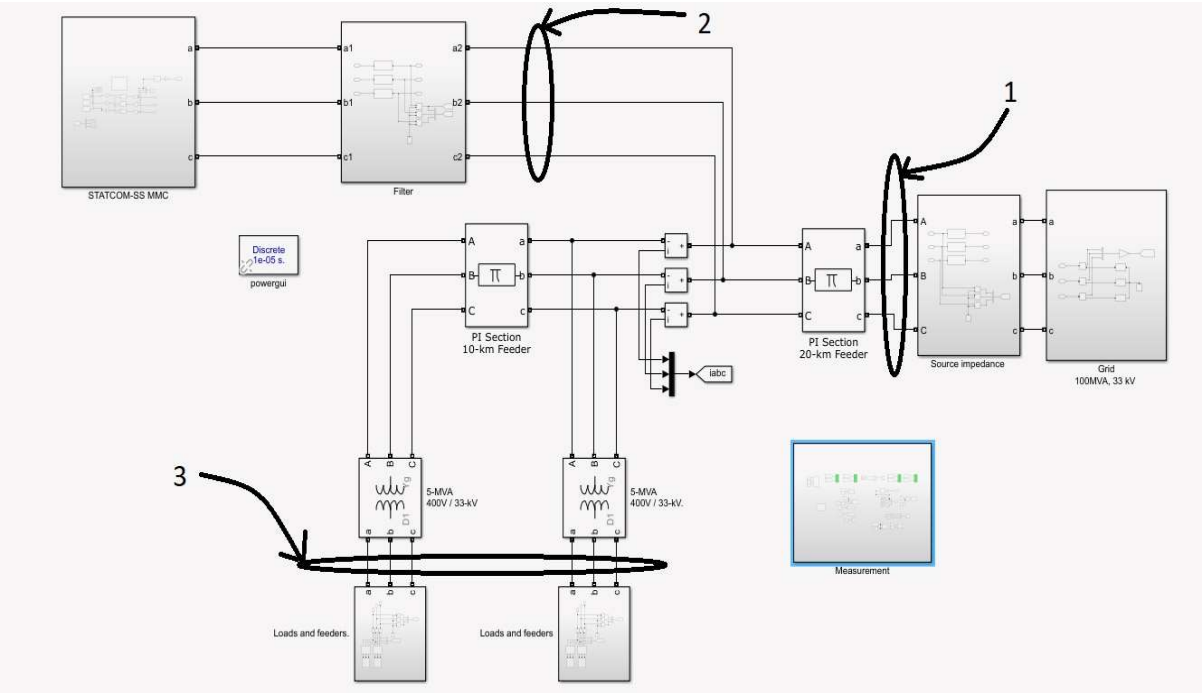

Fig. 5.18: The simulation model of the 33 kV distribution network

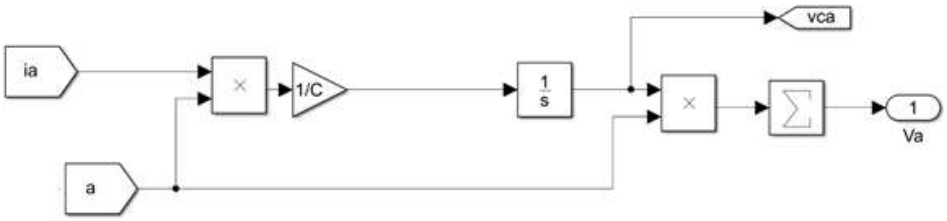

Fig. 5.19: The simulation model of the converter's leg

Fig. 5.20 shows the Matlab function of capacitor voltage-balancing algorithm for SMs within leg-a. When the leg current is charging the capacitors, the active SMs with the lowest capacitor voltages are turned on. On the other hand, the active SMs with the highest capacitor voltages are turned on if the leg current is discharging the capacitors. The number of active SMs can be easily calculated by adding the ones within an array. This array is obtained by comparing the modulating wave with the *m*-carrier signals as shown in Fig. 5.21. Fig. 5.22 shows the voltage profile of all capacitors. It is clear that, the balancing action is capable of balancing all the capacitors in terms of their voltages.

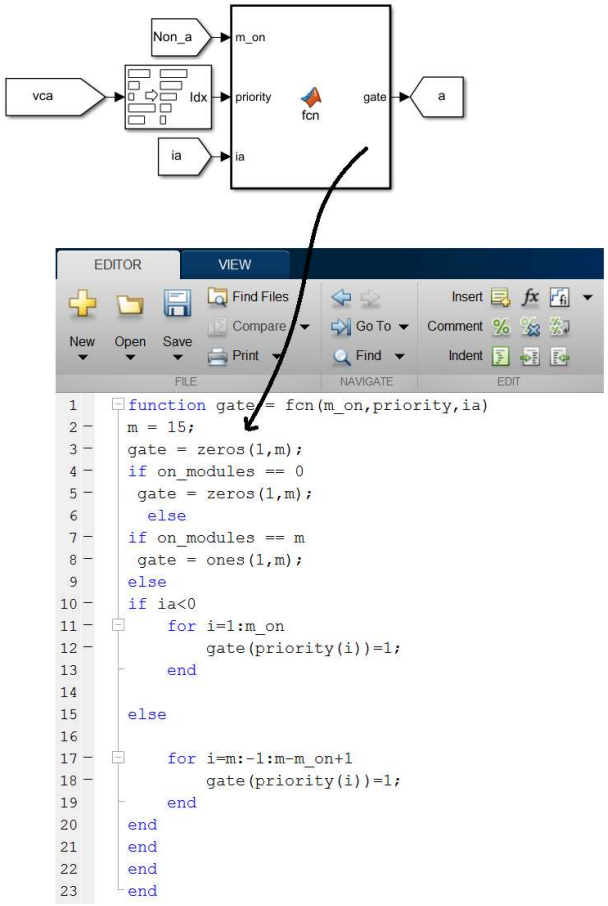

Fig. 5.20: The Matlab function of capacitor voltage-balancing algorithm for SMs within leg-a

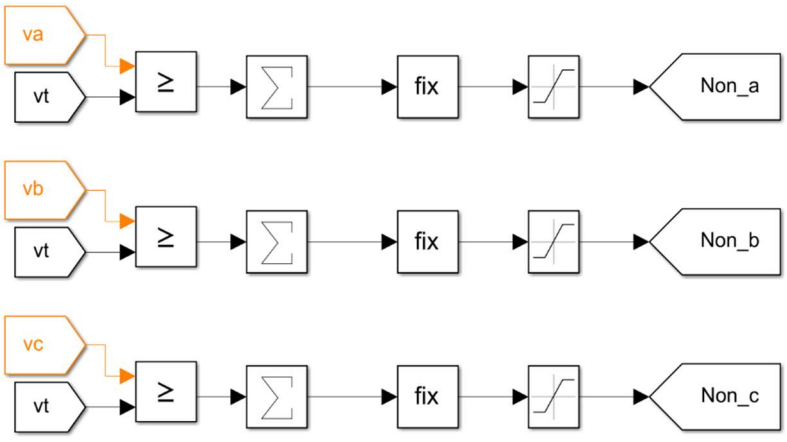

Fig. 5.21: The simulated model of the number of active SMs

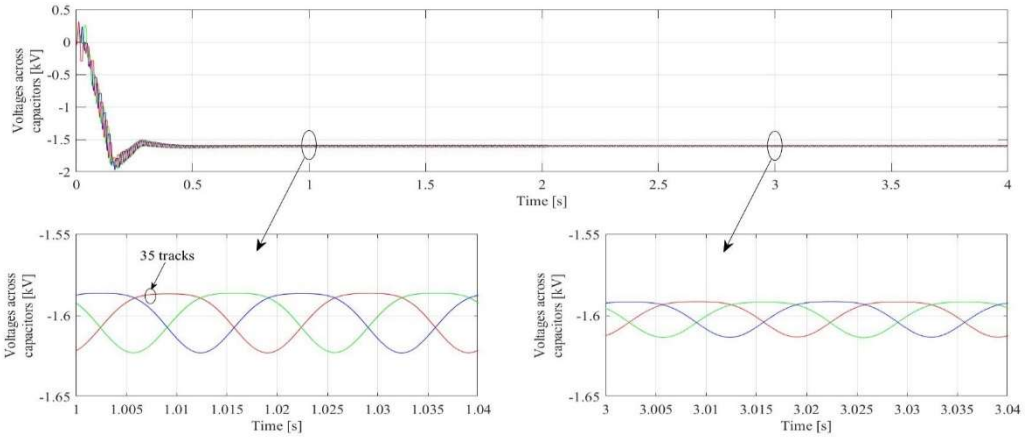

Fig. 5.22: The voltages across capacitors

Fig. 5.23 shows the converter's line voltages and line currents. It is clear that, the converter line currents are leading the voltages, which indicates that the proposed STATCOM is operating as a variable capacitor, and therefore the STATCOM feeds the distribution network with reactive power. When the step change in the power factor is applied to the loads (from 0.6 to 0.8 lagging), the voltage levels have been slightly reduced and the converter's line current decreases upon raising the power factor to generate the required reactive power to the loads and feeders.

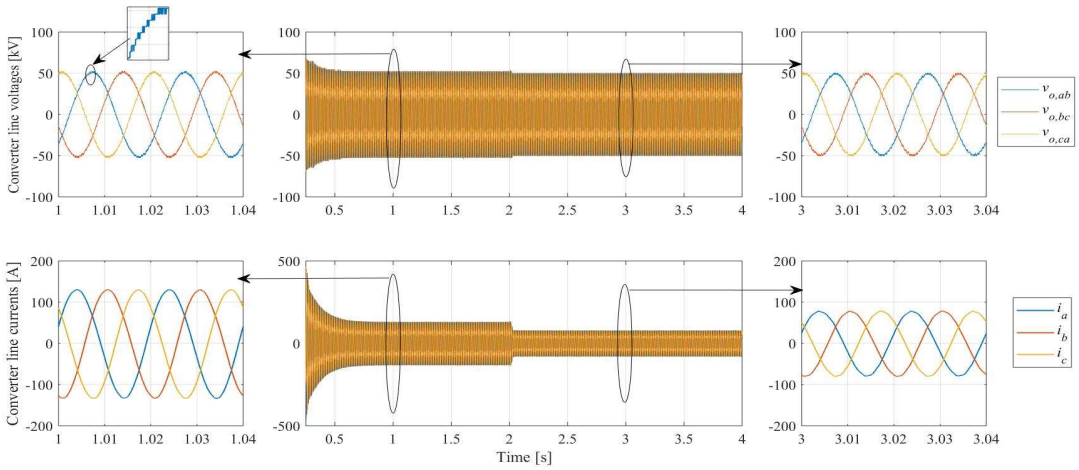

Fig. 5.23: The converter's line-to-line voltages and line currents of the 33 kV distribution network

Fig. 5.24 shows the average voltage across all capacitors and the voltage profile at the point of connection between the STATCOM and the distributed network. The results show a good capability of tracking the reference value of the capacitor average voltage (1.6 kV) and keeping the voltage of the distributed system at 33 kV (where Vc is calculated from equation 3.7; Vm= 33kV, M=1.15, m=35). The results also confirmed a stable operation of the proposed STATCOM even in the transient state at t = 2 s.

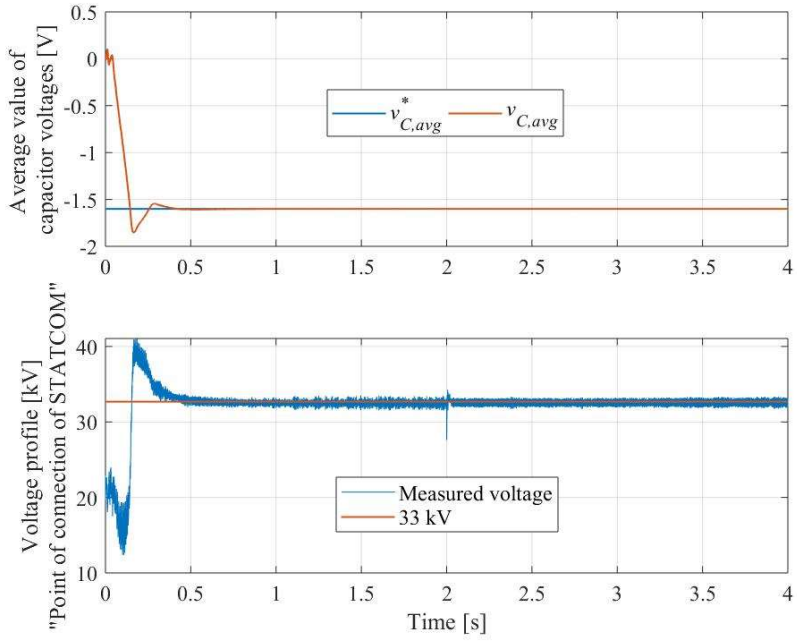

Fig. 5.24: The capacitive average voltage and the voltage profile at the point of connection of the STATCOM

Fig. 5.25 shows the *dq*-components of the converter's line currents. The reference quadrature component of the converter line currents has been set to a value, which is proportional to the reactive power absorbed by the loads, while the reference direct-axis component has been obtained from the DC voltage regulator. The results show a good capability of tracking the reference currents with a stable operation in the transient state at t = 2 s.

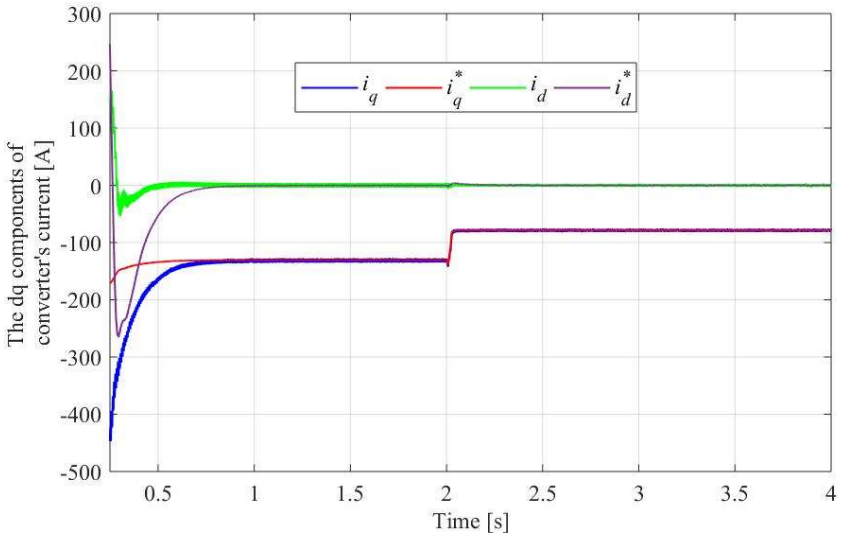

Fig. 5.25: The reference and measured *dq*-components of the converter's line currents

Fig. 5.26 shows the power measured at the grid (see indicator 1 in Fig. 5.18), the power measured at the converter (see indicator 2 in Fig. 5.18), the power absorbed by the loads (see indicator 3 in Fig. 5.18), and the grid's power factor. It clear that, the proposed converter is able to feed the total reactive power absorbed by the load in order to force the grid to feed the loads only with the required active power. As shown in the results, the active power absorbed by the loads is less than the expected value, which is the nominal rated power (6 MW for both loads) because the series RL-load is modelled on Matlab/Simulink using the relation between the nominal active power that has been specified on the parameters tab and the measured voltage that appears across the load. Therefore, both nominal active and reactive powers may be changed due to the voltage drop on feeders and transformers. As a result, the nominal power factor will be also changed (0.75 instead of 0.6 and 0.85 instead of 0.8).

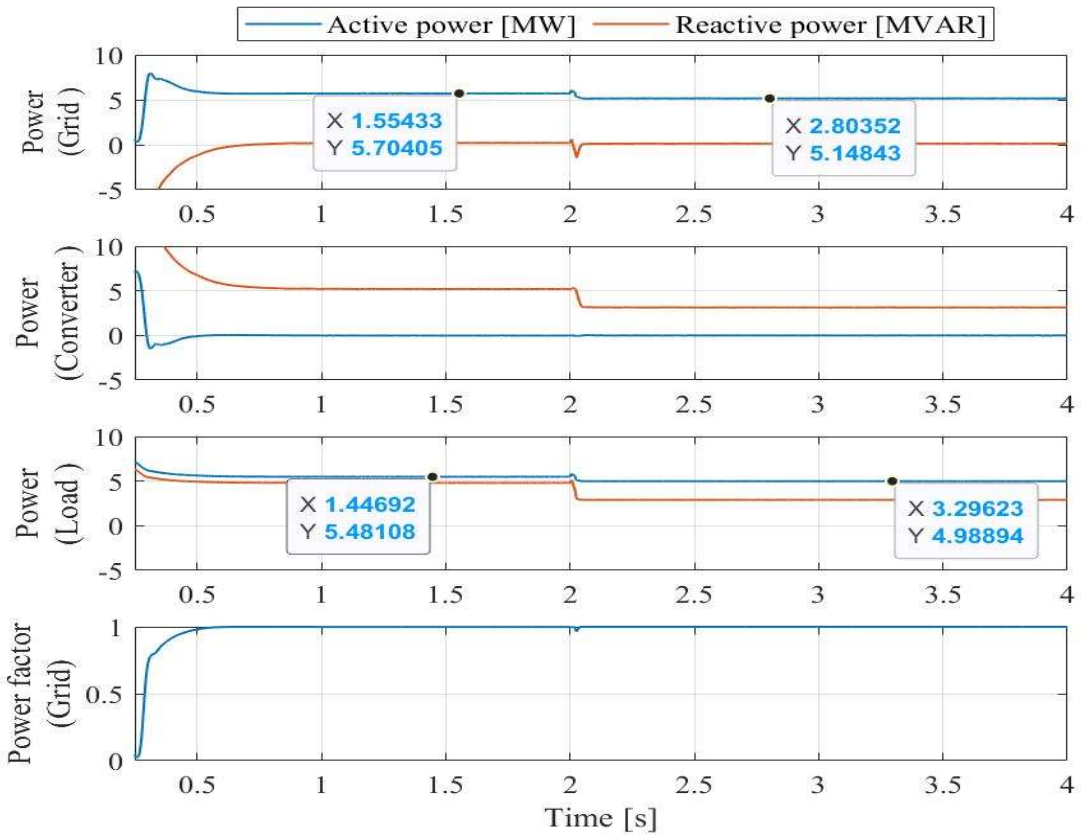

Fig. 5.26: The power generated by the grid, the power generated by the converter, the power absorbed by the loads, and the grid's power factor.

Fig. 5.27 presents the grid phase voltages and currents measured at the sending end of 20-km Feeder. It is worth noting that, the grid's phase currents and voltages are in phase and the grid is able to operate at a nearly a unity power factor.

Fig. 5.28 shows the grid's voltage profile and the grid's power factor with and without applying the STATCOM. It is clear that, the proposed converter is able to improve the voltage profile and run the grid at nearly unity power factor.

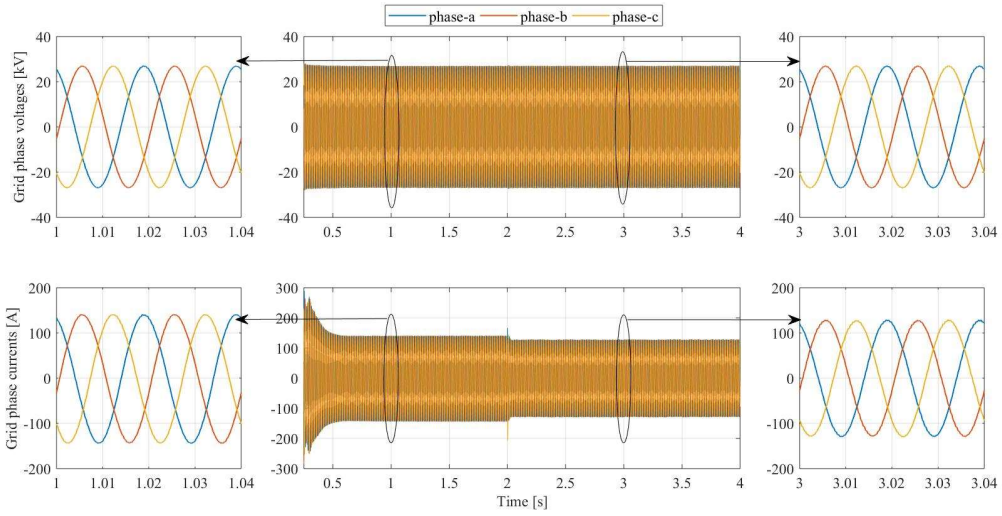

Fig. 5.27: The grid's phase voltages and currents measured at the sending end of 20-km Feeder

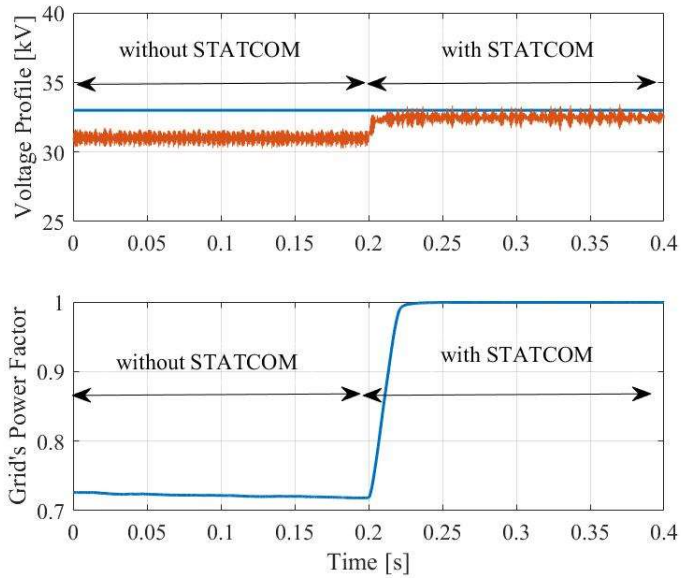

Fig. 5.28: The voltage profile and the grid's power factor with and without applying the proposed STATCOM

5.3 Reliability Assessment

The reliability of the proposed converter depends on the amount of reactive power generated to the load. If one of the SMs is damages in leg k (i.e, leg a), the converter can still operate properly to produce m levels instead of $m+1$ levels if one SM per each leg is bypassed taking into account the faulty module. If the rated reactive power of the converter is Q_r and the number of faulty modules in the leg is z, then the range of the output reactive power required is given by:

$$0 \le Q \le \left(\frac{m-z}{m}\right) Q_r , \tag{5.1}$$

Assuming that the IGBTs and diodes have the same static reliability where r_s is the reliability of each device, then the total reliability of the SM will be $r_s{}^4$ since each SM is designed using four devices. Therefore, the reliability of the proposed converter can be calculated as (using the theory on partial redundancy-Binomial Distribution) [16] :

$$R = \left(\sum_{i=z}^{m} \binom{m}{i} \left(r_s{}^4\right)^i \left(1 - r_s{}^4\right)^{m-i} \right)^3 , \tag{5.2}$$

On the other hand, the traditional two-level inverter consists of six IGBTs and six diodes. Therefore, the reliability of the converter is $r_s{}^{12}$ considering that the IGBTs and diodes have the same static reliability r_s [16].

In order to compare both reliabilities, the reliability of the SS-MMC has been compared with the reliability of the traditional two-level inverter, assuming m = 21 and r_s = 0.95. Fig. 5.29 illustrates both reliabilities versus the per unit reactive power. It is clear that, the proposed converter has a higher reliability for a wide range of generated reactive power (0 < Q < 0.73 pu). However, the reliability of the proposed converter decreases when the rated reactive power is required due to the reduction of the allowed number of faulty modules.

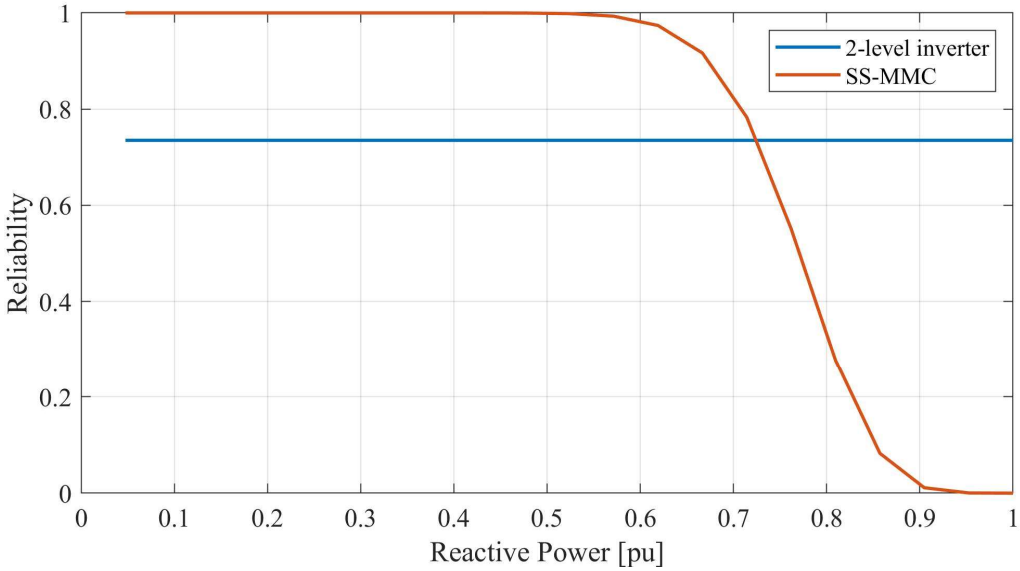

Fig. 5.29**:** The Reliability of the proposed converter versus two-level inverter (r_s = 0.95)

Chapter 6

Conclusions and Future Work

6.1 Conclusions

This thesis presents a new STATCOM for reactive power compensation based on modular multilevel converters. This topology integrates the capacitors in the power converter and produces an extremely low distortion of the output current. This thesis also presents detailed mathematical models for the control system including converter reactive power controller and grid synchronization. The proposed converter and the control algorithm including the current controller and the PLL have been tested by numerical simulation using a model of a static inductive load connected to the grid. The computer simulations in Matlab/ Simulink have confirmed the correct operation of the converter, and the results show that the modular multilevel converter topology can effectively ensure the operation at a unity power factor.

6.2 Future Work

While this thesis has demonstrated the potential of efficiently designing the modular multilevel converter with embedded capacitors for STATCOM applications, many opportunities for extending the scope of this thesis remain. The following research guidelines are suggested to be done in the future:

- Study the operation of the proposed converter under faulty conditions in SMs

- Implementing and designing the proposed converter practically on a small-scale laboratory prototype, the whole control system can be implemented and programmed using fast processor such as field programable gate array (FPGA).
- Verifying and testing the implemented converter to confirm the correct operation of the converter as a STATCOM

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